Effect of Fin Shape on GIDL and Subthreshold Leakage Currents

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Abstract

FinFETs have emerged as the solution to short channel effects at the 22-nm technology node and beyond. Here, the effect of fin shape on the leakage currents like Gate Induced Drain Leakage and subthreshold leakage is evaluated. The fin shape can be changed by varying the top width of the fin. Hence, the leakage currents are verified using their expressions for both rectangular and triangular FinFETs. The effects of oxide thickness, drain doping concentration and mobility on these leakage currents are also studied.

Keywords: FinFETs, Gate Induced Drain Leakage, Subthreshold leakage

I. INTRODUCTION

As device feature sizes enter the nanometre regime, leakage power consumption in VLSI systems has become one of the main barriers to technology scaling. Precise modeling of leakage current under process variations is crucial for the proper estimation of leakage power consumption and the optimal design of leakage-sensitive circuits. Double-gate FinFET transistors are recognized as one of the most promising successors of traditional planar bulk devices in the sub-50nm regime due to the significantly reduced leakage current, excellent short channel behaviour, and a fabrication process which is compatible with existing SOI or bulk technology processes. One of the major differences between a FinFET device and a planar device is the fact that the FinFET device consists of multiple small unit fins.

Minimization of transistor off-state leakage current is an especially important issue for low-power circuit applications. Leakage mechanisms include subthreshold leakage, gate oxide tunneling leakage, junction leakage, hot-carrier injection leakage, gate-induced drain leakage, and punch-through leakage currents.

A large component of off-state leakage current is gate induced drain leakage (GIDL) current, caused by band-to-band tunneling in the drain region underneath the gate when there is a large gate-to-drain bias, there can be sufficient energy-band bending near the interface between silicon and the gate dielectric for valence-band electrons to tunnel into the conduction band. GIDL imposes a constraint for gate-oxide thickness scaling because the voltage required causing this band-to-band tunneling leakage current decreases with decreasing gate oxide thickness, and GIDL can pose a lower limit for standby power in memory devices. GIDL current becomes less significant for digital logic applications as the power-supply voltage is reduced to below 1.1V (corresponding to the energy band gap of silicon); however, it is still an important consideration for applications such as dynamic random access memory (DRAM), for which data retention time is significantly degraded by GIDL current.

Subthreshold leakage current is the dominant mechanism in 90 nm and 65 nm technologies. It increases linearly as technology scales down. Subthreshold current, also known as weak inversion conduction current, between source and drain in a MOS transistor occurs when the gate voltage is below the transistor threshold voltage (Vth). The carriers move by diffusion along the surface, and there is an exponential relation between driving voltage on the gate and the drain current.

In this paper, fin shape significantly impacts leakage in bulk tri-gate nFinFETs with thin fin widths when the fin body doping is optimized to minimize leakage. Here, GIDL and subthreshold leakage current is observed when varying the fin shape. The various parameters that these leakage currents are depending are also studied.

The detailed description of GIDL and subthreshold leakage currents are presented in the first part of Chapter 2, followed by the description of processing of the fin-structures on bulk silicon wafers. Chapter 3 gives the analytical procedures of this project. Simulation results are discussed in Chapter 4. Finally, Chapter 5 gives the conclusion.
II. LITERATURE REVIEW

A. Sources of Leakage Currents:

Different physical phenomena contribute to the leakage currents causing the static consumption when one or more transistors in the $V_{dd}$ to $G_{nd}$ paths are in OFF-state. Figure 2.1 shows the contribution of different leakage currents in a transistor.

![Fig. 2.1: Leakage components in a transistor (Farzan Fallah et al., 2010)](image)

B. Gate Induced Drain Leakage (GIDL):

In some nanometric technologies, gate induced drain leakage current ($I_{GIDL}$) may appear. The carriers responsible for GIDL originate in the region of the drain that is overlapped by the gate. $I_{GIDL}$ is caused by the effects of high electric field in this region, when the gate is grounded and the drain is at $V_{dd}$. $I_{GIDL}$ current of an nMOS transistor flows from drain to the substrate.

![Fig. 2.2: Drain overlapped MOSFET: GIDL occurs in this region (“FinFETs and Other Multi-Gate Transistors”, by Jean Pierre Colinge)](image)

Several possible mechanisms contribute to this current. These include thermal emission, trap-assisted tunneling and band-to-band tunneling. It is the Band to Band Tunneling (BTBT) that has the MOSFET relevance at the voltages and structures of modern devices.

Consider a MOS structure as shown in figure 2.2. In the structure gate overlaps the drain junction. As gate becomes more negative or say drain becomes more positive at a fixed gate voltage then $p-n+$ junction become reverse biased. Due to reverse biased $p-n+$ junction, a depletion region forms near the drain junctions. Since the drain is heavily doped, the depletion region width formed inside the drain tends to be narrow, so band to band tunneling will start in this region, i.e. electrons tunnel from the valence band of $p$ region into conduction band of $n+$ region. The removal of electron from valence band produces a hole, which creates electron-hole pairs. Hence, a significant current flow can occur, called GIDL current (“Electronic Devices and Integrated Circuits”, by Singh).

![Fig. 2.3: Energy band curvature in the depleted drain region and electron tunneling from the valence band to the conduction band (“Physics of Semiconductor Devices”, by Jean Pierre Colinge and C. A. Colinge)](image)
This current may be further enhanced because the generated carriers are accelerated by the longitudinal electric field in the drain substrate junction and this causes impact ionization. For direct-band gap materials, $J_{GIDL}$ can be modelled by equation 2.1 ("FinFETs and Other Multi-Gate Transistors", by Jean Pierre Colinge).

$$J_{GIDL} = A \cdot E_{TOT} \cdot \exp \left( \frac{-B}{E_{TOT}} \right)$$  \hspace{1cm} (2.1)

Where, $A$ is a pre-exponential parameter given by equation 2.2 and $B$ is a physically-based exponential parameter given by equation 2.3 ("FinFETs and Other Multi-Gate Transistors", by Jean Pierre Colinge.). $E_{TOT}$ is the electrical field at point the maximum band-to-band tunneling.

$$A = \frac{2 \cdot q \cdot m_r \cdot \pi \cdot E_g^2}{h^3}$$  \hspace{1cm} (2.2)

$$B = \frac{\pi^2 \cdot m_r \cdot E_g^2}{q \cdot h \cdot 2^{\frac{3}{2}}}$$  \hspace{1cm} (2.3)

Where, $E_g$ is the energy band gap of the semiconductor channel and has a strong influence on the band-to-band tunneling current, $m_r$ is 0.2 * mass of electron, $q$ is the charge of electron, $h = h/2\Pi$, $h$ is the Planck’s constant. A large component of the $E_{TOT}$ is the surface electrical field $E_S$. $E_S$ is defined by equation 2.4 ("FinFETs and Other Multi-Gate Transistors", by Jean Pierre Colinge.).

$$E_S = \frac{V_{DG} - V_{FB} - E_{gap}}{\frac{\epsilon_{Si} \cdot \epsilon_{ox}}{t_{ox}}}$$  \hspace{1cm} (2.4)

Where, $V_{DG}$ is the drain to gate bias, $V_{FB}$ is the flat-band voltage, $E_{gap}$ is the energy band gap of silicon, $t_{ox}$ is the thickness of the oxide, $\epsilon_{Si}$ is the permittivity of silicon and $\epsilon_{ox}$ the permittivity of the oxide.

In a MOS transistor, if the gate voltage with reference to the source voltage ($V_{GS}$) is above the threshold voltage ($V_{th}$) then the dominant mechanism of the drain current is primarily drift based. Drift current is proportional to ($V_{GS} - V_{th}$)$^\alpha$ where $1 < \alpha < 2$. When the gate voltage is lower than the threshold voltage and there is a voltage applied between drain and source of a MOS transistor, the dominant mechanism of the drain current is primarily diffusion based. Diffusion current appears due to the different carrier concentration at the inversion layer in source and drain terminals. Figure 2.5 shows the subthreshold leakage current between drain and source. This current depends exponentially on gate-to-source voltage ($V_{GS}$) and drain-to-source voltage ($V_{DS}$) through the carrier concentrations ("Low Power CMOS Circuits and Technology, Logic Design and CAD Tools", by Christian Piguet).

In a long channel device, the depth of the depletion region in source and drain regions is relatively unimportant. As the channel length is reduced, these depletion regions occupy more space of the channel region. The depletion region near the source
and drain edges are shared with the channel. This effect produces a reduction of the threshold voltage when decreasing channel length and therefore, increases the subthreshold current ("Low Power CMOS Circuits and Technology, Logic Design and CAD Tools", by Christian Piguet).

D. Drain Induced Barrier Lowering (DIBL):

The Drain Induced Barrier Lowering effect consists of lowering the energy barrier between the source and the channel. This causes excess injection of the charge barriers into the channel and gives rise to an increased subthreshold current. Figure 2.6 presents the band diagram at the interface of the channel, for short and long channel transistors. At the interface, the channel consists of three regions: the source channel junction, the middle region, and the drain channel junction. For the long channel transistor, the energy bands in the central part of the channel can be taken to be approximately constant because the voltage almost drops at the drain channel junction. As the channel length is reduced, this situation is no longer true. Consequently, a reduction in the interface energy barrier occurs at the source channel junction where the maximum of the barrier is reached. This is the so-called DIBL effect. (T. A. Fjeldly et al., 1993).

Fig. 2.6: Physical origin of DIBL effect ("Low Power CMOS Circuits and Technology, Logic Design and CAD Tools", by Christian Piguet)

The magnitude of the subthreshold current is a function of the temperature, supply voltage, device size and the process parameters out of which the threshold voltage \( V_{\text{th}} \) plays a dominant role. For an nMOS transistor, the subthreshold current is given by equation 2.5 ("Low Power CMOS Circuits and Technology, Logic Design and CAD Tools", by Christian Piguet).

\[
I_{\text{sub}} = \mu_n \cdot C_{\text{ox}} \cdot \frac{W}{L} \cdot V_T \cdot \exp\left(\frac{V_{\text{GS}} - V_{\text{th}}}{n \cdot V_T}\right) \left(1 - \exp\left(-\frac{V_{\text{DS}}}{V_T}\right)\right) \tag{2.5}
\]

\[
V_T = \frac{k \cdot T}{q} \tag{2.6}
\]

\[
n = 1 + \frac{C_D}{C_{\text{ox}}} \tag{2.7}
\]

Where \( \mu_n \) is the electron carrier mobility, \( C_{\text{ox}} \) is the oxide capacitance per unit area, \( W \) is the channel width, \( L \) is the channel length, \( V_{\text{th}} \) is the threshold voltage, \( V_{\text{GS}} \) is the gate to source voltage, \( V_{\text{DS}} \) is the drain to source voltage, \( V_T \) is the thermal voltage given by the equation 2.6, \( T \) is the temperature in Kelvin, \( k \) is the Boltzmann constant, \( n \) is the inverse slope of the subthreshold current given by the equation 2.7 and \( C_D \) is the depletion channel region capacitance per unit area.

In short channel transistors, \( V_{\text{th}} \) is further modified as a function of the channel length and the drain-to-source bias and these are the so-called short channel and drain induced barrier lowering (DIBL) effects. Figure 2.7 shows the subthreshold leakage current when \( V_{\text{GS}} \) is less than \( V_{\text{th}} \).

Fig. 2.7: Drain current showing the subthreshold leakage current ("Physics of Semiconductor Devices", by Jean Pierre Colinge and C. A. Colinge)

E. FinFET:

The scaling of CMOS devices is moving towards the physical limits that can be achieved with the standard bulk technology. The off-state current and standby powers are increasing with shorter channel lengths. Since, it is becoming more difficult to keep the
electrostatic integrity of devices, channel doping needs to be increased and the source and drain junctions need to become shallower. But these trends are offset by the increased junction leakage and higher series resistances. Fully-depleted devices, double-gate devices in particular, offer significantly better electrostatic integrity and hence, better short-channel immunity. FinFETs are seen as the most likely candidate for the successor of the bulk CMOS from the 22 nm node onwards, because of its compatibility with the current CMOS technology. Many different ICs with FinFETs have already been demonstrated, ranging from digital logic, SRAM, DRAM to flash memory (“FinFETs and Other Multi-Gate Transistors”, by Jean Pierre Colinge).

Figure 2.8 shows the FinFET structure. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon “fin”, which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. The Wrap-around gate structure provides a better electrical control over the channel and thus helps in reducing the leakage current and overcoming other short-channel effects.

![FinFET structure](image)

**Figure 2.8: FinFET structure (A. Dixit, A. Kottantharayil et al., 2005)**

**F. Current Drive:**

In a multi-gate FET the current drive is essentially equal to the sum of the currents flowing along all the interfaces covered by the gate electrode. It is, therefore, equal to the current in a single-gate device multiplied by the equivalent number of gates (a square cross section is assumed) if carriers have the same mobility at each interfaces. For instance, the current drive of a double-gate device is double that of a single-gate transistor of equivalent gate length and width. In triple-gate and vertical double-gate structures all individual fins have the same thickness and width. As a result, the current drive is fixed to a single, discrete value, for a given gate length. To drive larger currents multi-fin devices are used. The current drive of a multi-fin MOSFET is equal to the current of an individual fin multiplied by the number of fins (also sometimes referred to as “fingers” or “legs”) (“FinFETs and Other Multi-Gate Transistors”, by Jean Pierre Colinge).

In the linear region, the current increases linearly with $V_{DS}$ when $V_{GS} > V_{th}$. To a first approximation, $I_{DS}$ in the linear region is given by the equation 2.9 (M. Zakir Hossain et al., 2011).

$$I_{DS} = 2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left( V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS}$$  

(2.9)

In the saturation region, $I_{DS}$ no longer increases as $V_{DS}$ and is given by the equation 2.10 (M. Zakir Hossain et al., 2011).

$$I_{DS} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \frac{(V_{GS}-V_{th})^2}{2 \cdot m}$$  

(2.10)

$$m = 1 + \frac{3t_{ox}}{x_{d}}$$  

(2.11)

Where $\mu$ is the effective mobility in the channel (inversion) region, $C_{ox}$ is the oxide capacitance per unit area, $W$ is the effective channel width, $L$ is the effective channel length, $V_{th}$ is the threshold voltage, $x_d$ is the depletion layer thickness and $t_{ox}$ is the oxide thickness.

**III. ANALYTICAL PROCEDURES**

In this project, the effect of fin shape on GIDL and subthreshold leakage currents has been studied. The fin shape normally in rectangular shape has been changed to triangular for better reduction in leakage currents. To change the fin shape, the width of the top of the fin has been changed while the bottom width remains unchanged.

**A. Effective Width Expression**

To compare different fin shapes, all $I_{ON}$ and $I_{OFF}$ values are normalized to the effective transistor width ($W_{eff}$). $W_{eff}$ is the component of the fin cross section perimeter adjacent to the gate oxide, calculated simply using the Pythagorean Theorem for the fin sides and the area of the semicircle with corner radius set to $W_{top}/2$ for the fin top and is given by the equation 3.1 (Brad D. Gaynor et al., 2014).
\[ W_{\text{eff}} = \sqrt{\left( \frac{W_{\text{bottom}} - W_{\text{top}}}{2} \right)^2 + \left( H - \frac{W_{\text{top}}}{2} \right)^2 + \frac{\pi W_{\text{top}}}{2}} \]  

(3.1)

Where, \( W_{\text{bottom}} \) is the bottom width of the active fin, \( W_{\text{top}} \) is the top width of the active fin and \( H \) is the fin height.

The key geometries shown in table 3.1 have been selected. The corner radius of the rounded fin is set to \( \frac{1}{2} W_{\text{top}} \) to minimize corner effects.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_{\text{bottom}} )</td>
<td>20nm</td>
</tr>
<tr>
<td>( W_{\text{top}} )</td>
<td>20nm for rectangular, 1nm for triangular</td>
</tr>
<tr>
<td>( H )</td>
<td>30nm</td>
</tr>
<tr>
<td>( L )</td>
<td>30nm</td>
</tr>
</tbody>
</table>

### B. GIDL Current Expression:

The FinFET GIDL current can be expressed by the equation (Farkhanda Ana et al., 2012),

\[ I_{\text{GIDL}} = W_{\text{eff}} \times L \times A \times E_{\text{TOT}} \times \exp \left( -\frac{B}{E_{\text{TOT}}} \right) \]  

(3.2)

\[ E_{\text{TOT}} = \sqrt{\left( \frac{(V_{DG} - V_{FB} - \psi_s)^2}{t_{ox}} \right)^2 + \frac{V_{DG}^2 \times \varepsilon_{ox}}{\varepsilon_{Si} \times t_{ox} \times H}} \]  

(3.3)

Where \( H \) is the parameter related to junction depth as,

\[ H = \frac{x_j^3 \times L^5 \times 10^{-4}}{t_{ox}^3} \]  

(3.4)

\( V_{FB} \) is the flat band voltage given by,

\[ V_{FB} = \Phi_m - \Phi_{Si} \]  

(3.5)

Where, \( E_{\text{TOT}} \) is the total electric field, \( A \) and \( B \) given by the equation 2.2 and 2.3, \( L \) is the length of the fin, \( \psi_s \) is the potential drop across silicon for band-to-band tunneling \( x_j \) is the junction depth, \( \Phi_m \) is the gate work function and \( \Phi_{Si} \) is the silicon substrate work function.

In case of GIDL current the values given to the different parameters are listed in the table 3.2. These values are given in the equation 3.2 inorder to calculate the GIDL current for various negative values of gate to source voltage.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_G )</td>
<td>Negative values</td>
</tr>
<tr>
<td>( V_D )</td>
<td>1 V</td>
</tr>
<tr>
<td>( t_{ox} )</td>
<td>2 nm</td>
</tr>
<tr>
<td>( A )</td>
<td>Pre-exponential constant</td>
</tr>
<tr>
<td>( B )</td>
<td>( 21.3 \times 10^8 ) ( \text{V/m} )</td>
</tr>
<tr>
<td>( x_j )</td>
<td>25 nm</td>
</tr>
<tr>
<td>( E_{cap} )</td>
<td>1.11 eV</td>
</tr>
<tr>
<td>( V_{FB} )</td>
<td>-0.9 V</td>
</tr>
</tbody>
</table>

### C. Subthreshold Current Expression:

The FinFET subthreshold current can be expressed by the equation (Giorgio Baccarani et al., 1999),

\[ I_{\text{sub}} = 2 \times \mu n \times C_G \times \left( \frac{W_{\text{eff}}}{L} \right) \times V_T^2 \times \exp \left( \frac{V_{GS} - V_{TH}}{V_T} \right) \left( 1 - \exp \left( -\frac{V_{DS}}{V_T} \right) \right) \]  

(3.6)

\[ C_G = \frac{C_{ox} \times C_D}{C_{ox} + C_D} \]  

(3.7)

\[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]  

(3.8)

\[ C_D = \frac{4 \times \varepsilon_{Si}}{t_{fin}} \]  

(3.9)

Where, \( \varepsilon_{ox} \) is the permittivity of the oxide, \( \varepsilon_{Si} \) is the permittivity of silicon and \( t_{fin} \) is the thickness of fin.
In case of subthreshold current the values given to the different parameters are listed in the table 3.3. These values are given in the equation 3.6 inorder to calculate the subthreshold current for various positive values of gate to source voltage.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS}$</td>
<td>Positive values</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>1 V</td>
</tr>
<tr>
<td>$T_{ox}$</td>
<td>2 nm</td>
</tr>
<tr>
<td>$\epsilon_{ox}$</td>
<td>3.9</td>
</tr>
<tr>
<td>$\epsilon_{Si}$</td>
<td>11.68</td>
</tr>
<tr>
<td>$t_{fin}$</td>
<td>5 nm</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>200 cm²/Vs</td>
</tr>
</tbody>
</table>

These equations for GIDL and subthreshold currents are computed and obtained the results using MATLAB.

**IV. RESULTS AND DISCUSSION**

The parameter values mentioned in the previous chapter are given to the equations 3.1- 3.9 corresponding to the two leakage currents GIDL and subthreshold current. The program is then run to obtain the 2D plots.

**A. Graphs for Drain Current in FinFET:**

The output characteristics of rectangular and triangular FinFET is obtained as shown in the figure 4.1.

Fig. 4.1: Output characteristics of both rectangular and triangular FinFET

For rectangular fin shape, the current is 510 $\mu$A/ $\mu$m and for triangular fin shape, it is 570 $\mu$A/$\mu$m, when $V_{GS}$ is equal to 0.6 volts. Hence, there is 11% increase in drain current when compared with rectangular fin shape. Figure 4.1 indicates that the drain current increases with increase in drain voltage and this condition is true up to pinch off voltage and beyond that there is no effect of drain voltage over drain current.

**B. Graphs for GIDL Leakage Current:**

GIDL current varying with negative values of gate voltage for both rectangular and triangular fin shape is obtained in the figure 4.2.

Fig. 4.2 GIDL characteristics of both rectangular and triangular FinFET
For rectangular fin shape, the current is 31 µA/m and for triangular fin shape, it is 27 µA/m at -4 volts. Hence, there is 13% decrease in leakage current when compared with rectangular fin shape.

The GIDL leakage current is compared by varying oxide thickness in both rectangular and triangular FinFET as shown in figure 4.3. It is clear that by increasing the oxide thickness the current can be reduced in both rectangular and triangular FinFET.

![Fig. 4.3: GIDL characteristics for varying oxide thickness](image)

The GIDL leakage current is also compared by varying junction depth in both rectangular and triangular FinFET as shown in figure 4.4. It is clear that by increasing the junction depth the current can be reduced in both rectangular and triangular FinFET.

![Fig. 4.4: GIDL characteristics for varying junction depth](image)

The comparison of GIDL current in both rectangular and triangular FinFET with different drain doping concentration has also being compared and is shown in figure 4.5. From the graph we can infer that by decreasing drain doping concentration the current can be reduced.

![Fig. 4.5: GIDL characteristics for varying drain doping concentration](image)

The results can be tabulated as in table 4.1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Rectangular FinFET</th>
<th>Triangular FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide thickness</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 nm</td>
<td>0.35 nA</td>
<td>0.3 nA</td>
</tr>
<tr>
<td>1.5 nm</td>
<td>0.52 nA</td>
<td>0.47 nA</td>
</tr>
<tr>
<td>Junction depth</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 nm</td>
<td>0.16 nA</td>
<td>0.14 nA</td>
</tr>
<tr>
<td>25 nm</td>
<td>0.32 nA</td>
<td>0.28 nA</td>
</tr>
<tr>
<td>Drain doping</td>
<td></td>
<td></td>
</tr>
<tr>
<td>concentration 5*10^30</td>
<td>0.53 nA</td>
<td>0.46 nA</td>
</tr>
<tr>
<td>5*10^20</td>
<td>0.047 nA</td>
<td>0.042 nA</td>
</tr>
</tbody>
</table>

The results can be tabulated as in table 4.1.
So, the GIDL current can be reduced by decreasing the drain doping concentration, increasing the oxide thickness and also by increasing the junction depth. These effects are also applicable to rectangular as well as triangular fins. i.e., by changing from rectangular to triangular the leakage current is further lowered.

C. Graphs for Subthreshold Leakage Current:

GIDL current varying with positive values of gate to source voltage for both rectangular and triangular fin shape is obtained in the figure 4.6.

For rectangular fin shape, the current is 8.5 \(\mu\text{A}/\text{m}\) and for triangular fin shape, it is 7.5 \(\mu\text{A}/\text{m}\) at 0.4 volts. Hence, there is 12\% decrease in leakage current when compared with rectangular fin shape.

The subthreshold leakage current is compared by varying oxide thickness in both rectangular and triangular FinFET as shown in figure 4.7. It is clear that by increasing the oxide thickness the current can be reduced in both rectangular and triangular FinFET.

The comparison of subthreshold current in both rectangular and triangular FinFET with different mobility has also being done and is shown in figure 4.8. By decreasing mobility, the current can be reduced.
The leakage current with respect to temperature is also plotted showing that the current is lower in triangular fin when compared to rectangular fin. In case of rectangular fin, the current is 105µA/m and for triangular fin it is 95µA/m at 400K i.e., 10% decrease in current. The results can be tabulated as in table 4.2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Rectangular FinFET</th>
<th>Triangular FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide thickness</td>
<td>2 nm</td>
<td>.15 mA</td>
</tr>
<tr>
<td></td>
<td>1 nm</td>
<td>.29 mA</td>
</tr>
<tr>
<td>Effective mobility</td>
<td>670 cm²/Vs</td>
<td>.45 mA</td>
</tr>
<tr>
<td></td>
<td>220 cm²/Vs</td>
<td>.15 mA</td>
</tr>
</tbody>
</table>

However, to reduce the subthreshold leakage current, the oxide thickness need to be increased and the effective mobility need to be decreased. These effects are also applicable to rectangular as well as triangular fins. i.e., by changing from rectangular to triangular the leakage current is further lowered.

**V. CONCLUSION**

Double-gate FinFET devices are considered as one of the most promising successors of conventional MOSFET devices. Due to the physical fin structure, the width of a FinFET device can be changed. Here, the impact of fin cross-section shape on bulk trigate nFinFETs with thin fins is evaluated. It is clear that the fin shape has considerable impact on leakage performance. With appropriate doping optimization, a 22-nm nFinFETs with triangular fin cross section results in more than 10% reduction in leakage current over a rectangular fin with the same base fin width.

Here, the effect of fin shape on various device parameters like oxide thickness, drain doping concentration, effective mobility, junction depth and temperature is also explored and showed that, all these parameters affects the leakage currents like GIDL and subthreshold more in the case of triangular FinFET. MATLAB 8.3 has been used for the verification of the results. However, future research is needed to further reduce the leakage current in bulk FinFETs.

**VI. REFERENCES**


