Design of Low Power Pulse Triggered Flip-Flops

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Abstract

In digital CMOS design, power consumption has been a major concern for the past several years. Advanced IC fabrication technology allows the use of nano-scaled devices; so the power dissipation becomes the major problem. Flip-flops are widely used in many sequential logic circuits such as registers, memory elements, counters, etc. These circuits are widely used in the implementation of VLSI chips. Therefore the power consumption of such circuits should be improved, without deteriorating other characteristics. Pulse-triggered FF has a simple circuit which lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are narrow, then the latch acts like an edge-triggered FF.

Keywords: Flip-Flop, latch, power, and pulse triggered

I. INTRODUCTION

Latches and flip-flops are the basic building blocks of synchronous digital circuits and to a large extent determine circuit speed and power consumption. Their performance is affected by clocking strategy of the circuits. In recent VLSI's, a clocking system, including clock interconnections and Flip-Flops,(F/F), consumes 20'%0 to 45'%0 of the total chip Power. This is partially because the activation ratio of a clock system is unity. In this clocking system power, 90% is consumed by the last branches of the clock distribution network which drive directly F/Fs and the F/Fs themselves. In order to achieve low-power VLSI's, it is important to reduce the clocking system power. A flip flop or latch is a circuit that has two stable states and can be used to store state information. They are used for storage of states (0 or 1).

Master-slave flip-flops, sense amplifier based flip-flops and pulsed-triggered flip-flops are used in many existing microprocessors. Master-slave flip-flops consist of two stages, one is master and another one is slave and they are characterized by their hard-edge property [7] [10]. Master-slave flip-flops and sense amplifier based flip-flop are characterized by positive setup time, causing large D-to-Q delays. On the other side, pulse-triggered flip-flops reduces the above two stages into one stage and is characterized by the soft edge property and a negative setup time, resulting in small D-Q delay [7] [10]. Pulse-triggered flip-flops can be classified into different types of flip-flops. Based on the pulse generators used, pulse-triggered flip-flops can be categorized into two types as: implicit-pulsed and explicit-pulsed. Pulse triggered flip-flops can be static, or semi-static, or dynamic, or semi-dynamic. Pulse-triggered flip-flops can also be classified into single-edge triggered flip-flops and double-edge triggered flip-flops. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop, example, hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO). Whereas, in explicit-pulse triggered flip-flops (ep-FF) the pulse is externally generated, for example, explicit-pulse data-close-to-output flip-flop (ep-DCO) [7] [10] [1].

After the detailed study of it is observed that researchers have designed various conventional types of flip-flops that optimizes area, delay, power and large discharging path problem. Their related work has been mentioned below:

Jin-Fa Lin has proposed external type pulse low power flip-flop and modified true single phase clock latch using 90 nm CMOS technology which is based on a signal feed-through scheme. In this paper first they have compared and discussed about some flip-flops such as ep-DCO, CDFF, Static-CDFF, MHLFF. Drawbacks of this flip-flop were long discharging path problem, longer delay and larger switching power dissipation.

He proposed a low-power P-FF design based on a signal feed-through scheme consisting of a pass transistor and pseudo-nMOS logic. His design managed to reduce the delay in latching the data "1" and "0," and also reduced the longer delay by feeding the input signal directly to an internal node of the latch design which speeds up the data transition [1].

Saranya. L *et al.* have designed Low-Power Pulse-Triggered flip-flops. They studied and designed three different kinds of conventional pulse-triggered flip-flops. The implicit Pulsed Data-Close to output pulse-triggered flip-flop, the Modified Version of Hybrid latch flip-flop and the Single-ended Conditional Capturing Energy Recovery flip-flop. Their design carried out comparison of low power pulse triggered flip-flops between SAL, SVL logics and they obtained the best power -delay-performance [2].

Tania Gupta *et al.* paper have designed dual edge triggered flip flop. They compared three existing designs of dual edge triggered flip-flop such as EP_CDFF, EP_CPFF and DET-SAFF with the proposed design of the dual edge triggered flip-flop (DET-FF). In EP_CDFF type of design included pulse generator and conditional discharge. The pulse generator is used to produce the dual pulse which is active at both rising and falling edge of the clock. Conditional discharge technique is used to

reduce the unnecessary charging and discharging of the internal major nodes when the input is same for the long time, which leads to the power consumption. In EP_CPFF type of design includes conditional pre-charge technique for removing the redundant transitions of the flip-flop to reduce the power dissipation. In DET-SAFF type of design sense amplifier is used for flip-flop design [3].

Sayed Alireza Sadrossadat *et al.* have proposed a statistical design of the flip-flops circuits to achieve a high yield, to meet the performance, leakage power, switching power, and layout area design specifications using 45 nm CMOS technology. Their proposed design provides solution for design parameters such as width and length of the flip-flop transistors, which provide maximum immunity to the process variations in the transistor dimensions and threshold voltage. The proposed design showed that for a given flip-flop design specifications, the flip-flops have to be designed using statistical sizing tools to improve the timing yield [5].

Massimo Alioto *et al.* have compared a large number of FFs i.e., 19 topologies belonging to four different classes in 65-nm CMOS technology. The comparison has been performed on the basis of whole energy-delay-area design space. The other parameters considered for comparison were layout parasitic, leakage in both standby and active mode, wide load and switching activity.

According to their analysis, the fastest topology is the STFF, the best low-energy FFs are the DETTGLM and TGFF, whereas the most energy-efficient TGPL [6].

II. CONVENTIONAL FLIP-FLOPS:

A. Explicit Type Flip-Flop (Ep-DCO):

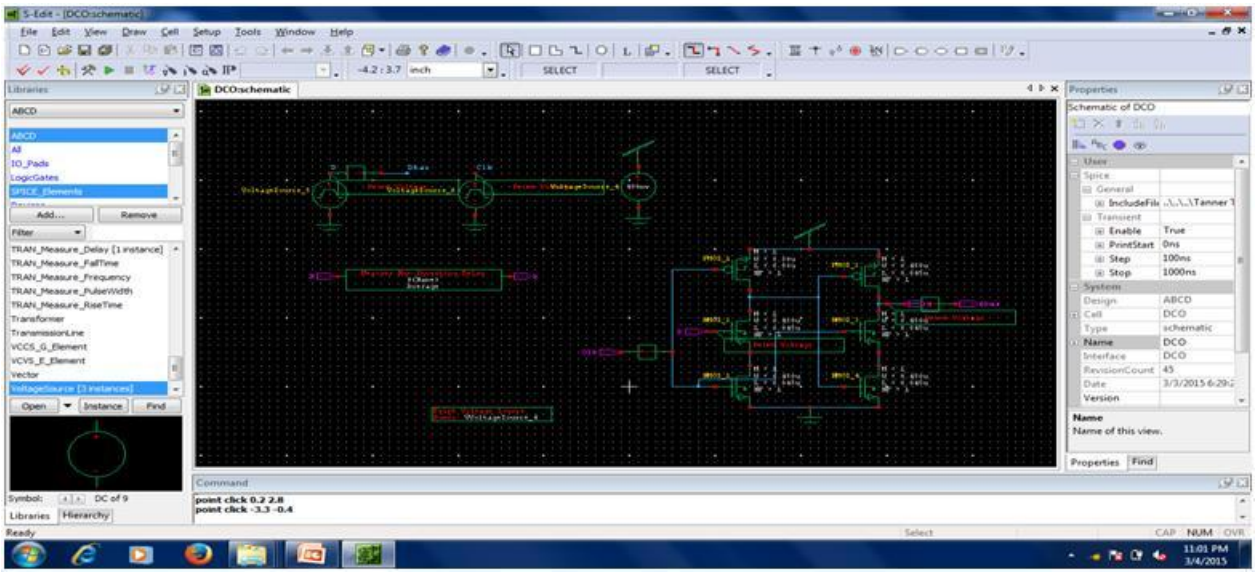

Fig. 1: Ep-DCO Schematic using In Tanner Tool

It contains a NAND logic-based pulse generator. Amount of power consumed by charging and discharging the internal node X high. Glitches appear at the output that would cause noise problem. The internal node X is discharged on every rising edge of the clock. This gives rise to large switching power dissipation.

B. Conditional discharge flip-flop:

CDFF operates in two stages. The first stage is LOW to HIGH transition, and the second stage is HIGH to LOW transition. This FF faces a worst case delay caused by a discharging path consisting of three stacked transistors.

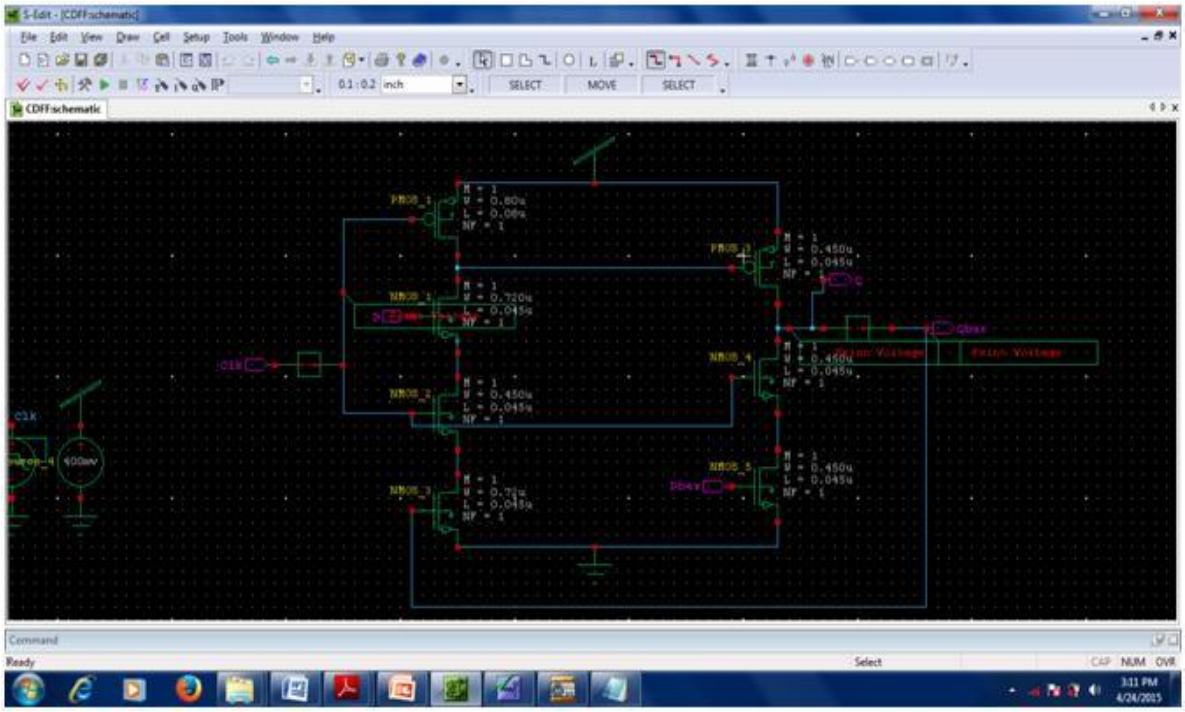

Fig. 2: CDFF Schematic using in Tanner Tool

C. SCDFF: Static- conditional discharged Flip-Flop:

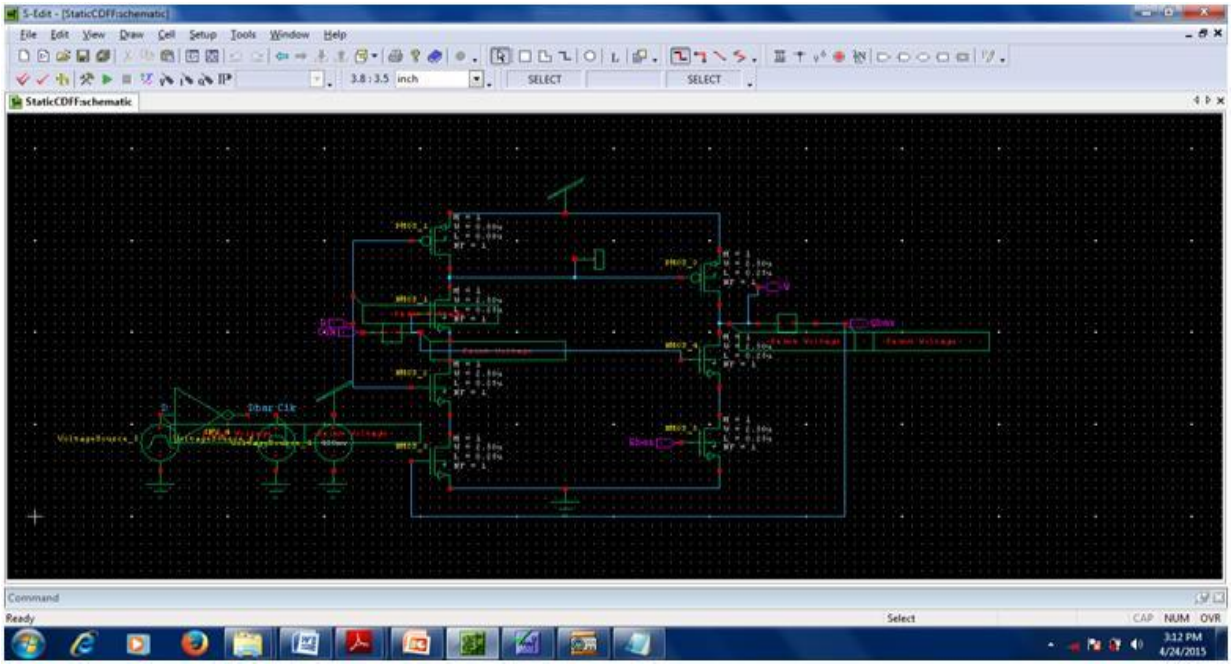

Fig. 3: SCDFF Schematic using In Tanner Tool

Above design shows a similar P-FF design using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. It shows that a longer data-to-Q (D-to-Q) delay is less than the CDFF design.

III. PROPOSED PULSE-TRIGGERED FLIP-FLOP

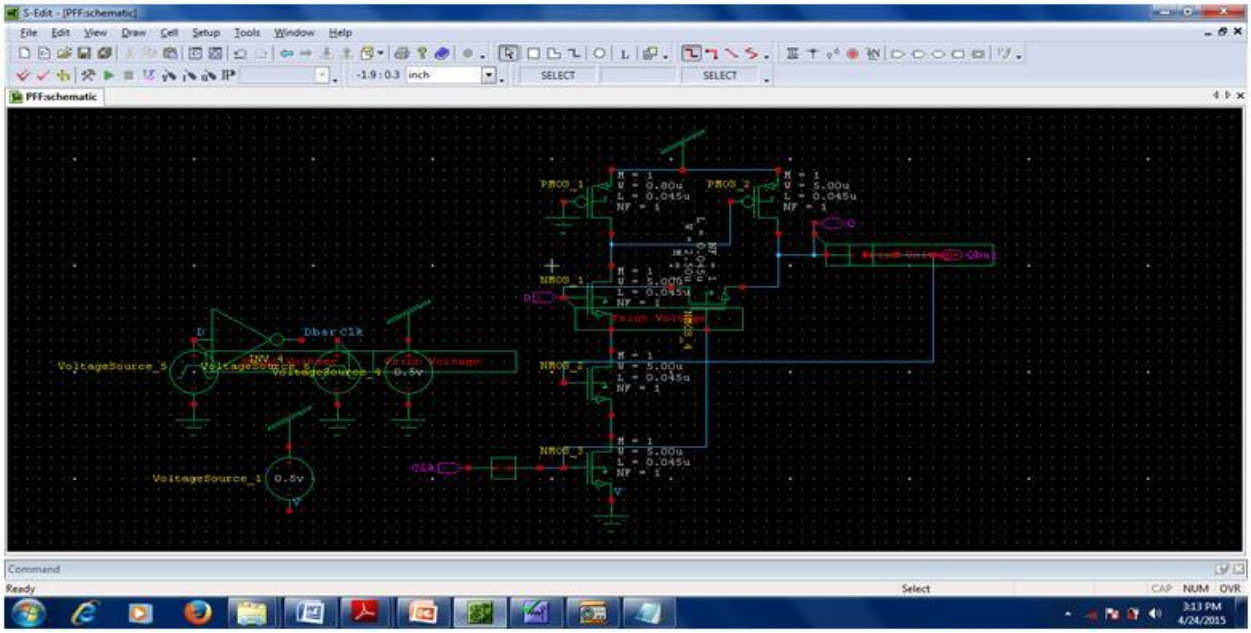

Fig. 4: Pulse Triggered Ff Schematic Using in Tanner Tool

By studying the various conventional type flip-flops it is observed that there are some drawbacks regarding these flip-flops as belows:

- Power consumption at the internal node is high.
- Glitches appear at the output that would cause noise problem.
- Discharging occurs on every rising edge of the clock.
- Large switching power dissipation.
- Delay caused by a discharging of stacked transistors.
- Longer Data-to-Q (D-to-Q) delay during '0' to '1' transitions.
- Internal node becomes floating when output and input Data both are equal to 1.

To overcome the above drawbacks we implemented pulse triggered flip-flop that avoids switching at an internal node, improves the "0" to "1" delay and reduces the difference between the rise time and the fall time.

IV. SIMULATION RESULTS

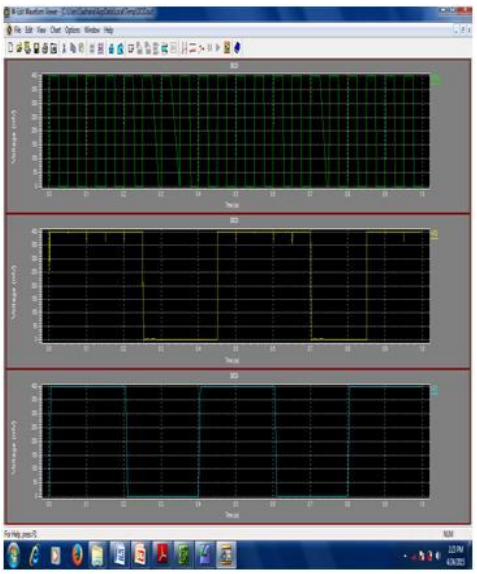

Fig. 5: Simulation output for EP-DCO using Tanner Tool

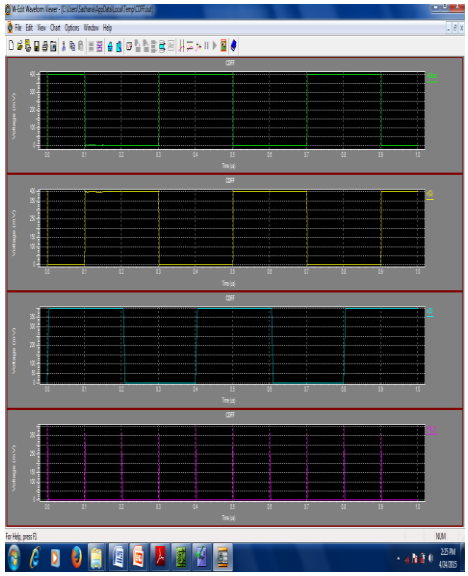

Fig. 6: Simulation output for CDFF using Tanner Tool

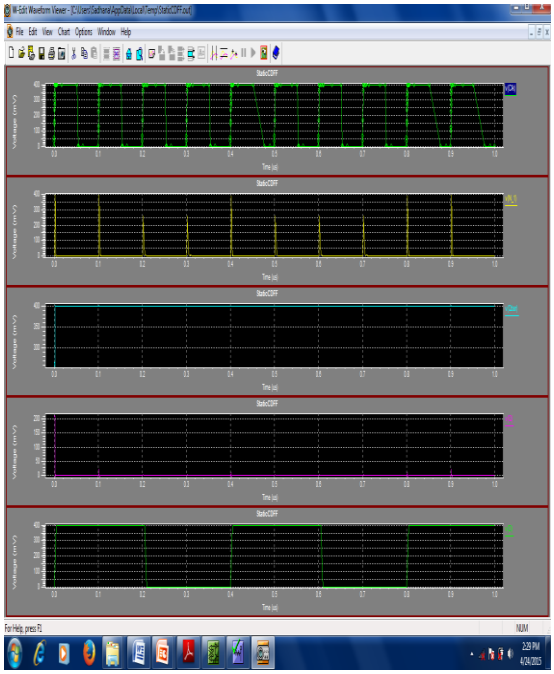

Fig. 7: Simulation Output for SCDFF using Tanner Tool

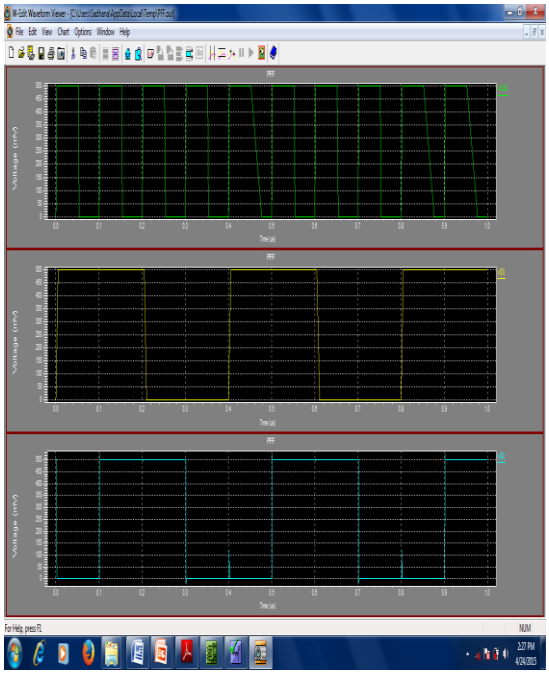

Fig. 8: Simulation Output for Pulse Triggered FF using Tanner Tool

Table-1:
Comparison between Different Values

Type of Flip-Flops	*EP-DCO*	*CDFF*	*SCDFF*	*P-FF*
Transistor Count	*24*	*28*	*29*	*24*
Average Power Consumed	*0.381uW*	*0.39uW*	*0.435uW*	*0.0876uW*
Delay	*0.146us*	*0.0532us*	*0.0574us*	*0.05378us*

V. CONCLUSION

In this paper, a pulse triggered flip-flop for delay and power reduction is proposed. Simulation results indicate that the proposed Flip-flop design excels conventional flip-flop designs in its performance metrics such as average power consumption, minimum D-to-Q delay and transistor count.

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