Design and Analysis of Low Voltage Low Dropout Regulator (LDO)

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Abstract

In battery operated portable devices, handheld devices and noise sensitive devices which need high precision supply voltages has fuelled the expansion of Low Drop-Out Regulators. Low-Voltage Low-Dropout(LDO) Voltage Regulator that can operate with a very small Input–Output Differential Voltage with nm CMOS technology which improves package density. Now-a-days, design of Low Drop-Out Regulators with high performance is challenging problem. The demand of LDO is increasing because of growing demand of portable electronic devices like cellular phones, pagers, camera recorders and laptops. In this paper, Design and Analysis of Low Voltage Low Dropout Regulator is proposed. The proposed circuit is simulated using 45 nm CMOS technology process parameters and the simulation results are presented. The simulation of proposed circuit is designed using ADS i.e. Advance Design System tool. The proposed LDO gives output voltage near about 0.8V from a 1V supply, and dropout voltage near about 200mV using a reference voltage of 0.4V.

Keywords: Low-dropout (LDO) regulator, low-voltage, Low Quiescent Current, Power Supply Rejection Ratio, Area, 45nm CMOS Technology etc.

I. INTRODUCTION

Low-dropout regulators (LDO) are widely used in electronic products due to their precision output voltage and a smaller amount prone to noise. In designing of LDOs, stability is an important issue. Low dropout regulator (LDO) is an important building block in power management. It provides constant output voltage. LDO often follows DC-DC converter. A low dropout regulator is a class of linear regulator. A linear voltage regulator operates at a small input-output differential voltage is called as low dropout voltage regulator. Conventional LDO regulators usually consist of an error amplifier (differential amplifier), a voltage reference, a feedback voltage divider, and a pass transistor. The output current flows through pass transistor and its gate voltage is controlled by error amplifier. This output compares the reference voltage with the feedback voltage, amplifying the difference so as to reduce the error voltage. Low dropout regulators can be categorized as either low power or high power. The advantages of a low dropout voltage include a lower minimum operating voltage, higher efficiency operation and lower heat dissipation.

Due to increasing demand of high performance LDOs it become more challenging. There are some requirements of the regulator, such as line regulation, load regulation, and transient response. There are several techniques for designing low dropout (LDO) regulator like Enhanced active feedback technique with dynamic compensation, adaptive Miller Compensation, NMOS power transistor and dynamic biasing technique, Current buffer compensation, Feed-Forward Ripple Cancellation.

Low-dropout regulators (LDOs) are most widely used power supply modules for noise-sensitive analog. LDO regulators are used in many applications like automotive, power management and industrial areas, which requires a low dropout voltage for its proper functioning. LDOs are also used in camera, laptops, and mobile phones which uses Bluetooth and Wireless frequency applications.

In today’s real world VLSI is in very much demand. After the careful study of reported work it is observed that researchers have taken a work for designing LDO with CMOS technology. The related works have been mentioned as follows:

Ying-Ting Ma et al. have proposed low voltage low dropout regulator. The proposed LDO implemented in 90nm CMOS technology. To boost the gain a simple symmetric operational transconductance amplifier is used as the error amplifier (EA), by means of a current splitting technique. Due to rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed which minimizing the size of the power MOS transistor. A Fast responding transient accelerator is designed from the reuse parts of the error amplifier (EA). The advantage of proposed LDO regulator is to operate over wide range of operating condition and achieving 99.94% current efficiency. The proposed architecture minimizes area of LDO [1].

Chia-Min Chen et al. have proposed low voltage dropout regulator by using a novel frequency compensation technique. The LDO regulator was designed using TSMC 0.35-µm CMOS technology. The proposed LDO employ Enhanced active feedback frequency compensation to improve the frequency response. Stability of proposed LDO achieved using Enhance active feedback loop techniques and embedded RC blocks can be achieved with or without loading capacitors. The proposed LDO regulator adopts both a feed forward path and a fast path to achieve fast load transient responses and small overshoots and undershoots. The LDO design provides large loop gain to improve line and load regulation. The proposed LDO provides low quiescent current and high speed transient response [2].

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Ho-Joon Jang et al. have proposed LDO regulator with improved PSR at high frequency. The proposed LDO implemented in 0.13 μm CMOS technology. The power supply rejection (PSR) of low drop-out (LDO) voltage regulator is improved by employing an error amplifier (EA) which is configured so the power supply noise is cancelled at the output. The EA of the LDO regulator is composed of multiple stages which are designed so the noise of the external power supply line can be cancelled and does not appear at the output. The noise of the external power supply line can be rejected if the exactly the same amount of noise can be coupled to the gate of power transistor. The power supply rejection of a linear LDO regulator is improved by configuring the error amplifier so the power supply noise can be cancelled at the output [3].

M. El-Nozahi et al. have proposed feed forward ripple cancellation technique for designing LDO. This technique provides high power supply rejection over wide range of frequency. By using 0.13μm CMOS technology is used for designing LDO. There are some techniques used for improving PSR like i) Using simple RC filtering at the output of the LDO ii) Cascading two regulators iii) Cascading another transistor with the PMOS pass transistor along with RC filtering but to improve PSR at high frequency they use feed forward ripple cancellation technique. By using feed forward amplifier and summing amplifier the fees forward path is established. Advantage of this technique is high PSR without increasing the loop bandwidth for wide range of frequency and hence quiescent power consumption. Ideally feed forward path does not affect stability of LDO because feedback path is not there. Kelvin connection is used to improve gain bandwidth product. This technique provides robust design when process, temperature and bonding inductance variation is considered. They have proposed LDO in 0.13μm CMOS technology, achieving PSR of -56 dB at 10 MHz frequency [4].

Robert J. Milliken et al. have proposed an external capacitor less LDO architecture. The large external capacitor used in typical LDOs is removed allowing for greater power system integration for system-on-chip (SOC) applications. A compensation scheme is presented that provides both a fast transient response and full range alternating current (ac) stability. The LDO regulator has been fabricated in 0.35 μm CMOS technology [5].

II. SPECIFICATION OF LDO

The important aspects of the LDO can be summarized into three categories, namely, regulating performance, quiescent current flow, and operating voltages. Some specifications for the LDO include drop-out voltage, line regulation, load regulation, Power supply rejection ratio (PSRR) [6].

A. Dropout Voltage:

Drop-out voltage is the “minimum voltage difference” between input and output voltages of LDO at which the output voltage is still regulated. In proposed LDO architecture can be seen that when VDD is small, the output voltage is no longer regulated to a fixed value. In low-VDD operating region, it is usually called as “dropout mode”. The drop-out voltage is mainly related to the architecture of the error amplifier and the output pass transistor.

B. Quiescent Current:

Quiescent current is also called as ground current. It is the difference between the input current and the output current. To maximize current efficiency quiescent current should be low. Quiescent current consists of bias current and the gate drive current of the series pass element. Generally value of quiescent current can be determined by the series pass element, topologies, ambient temperature, etc.

C. Transient Response:

The transient response is the maximum allowable output voltage variation for a load current step change. The transient response is a function of the output capacitor value, equivalent series resistance (ESR) of the output capacitor, the bypass capacitor that is usually added to the output capacitor to improve the load transient response, and the maximum load-current.

D. Power Supply Rejection Ratio (PSRR):

PSRR means the ability of LDO to reject ripple it sees at its input. It is given by

$$\text{PSRR} = \frac{\Delta V_{DD}/\Delta V_{OUT}}{V} \text{ (dB)}$$

Low drop-out regulators use a feedback loop to keep a stable output voltage. With any feedback loop there is phase shift around the loop and the amount of phase shift determines loop stability of LDO. To have a constant loop the phase shift around the (open) loop must always be less than 180° (lagging) at the point where the loop has unity gain, or 0 dB. There is different compensation techniques which can provide stable operation of LDO depending on topology used.
III. PROPOSED REGULATOR ARCHITECTURE

The LDO is designed to optimize its Four Parameter:
- Transient Response
- Quiescent current
- PSRR
- Low Voltage Operations

The schematic of proposed LDO is shown in fig 1. The first part contains the Operational Transconductance Amplifier (OTA) which works as Error Amplifier, which is composed of M_{EA1}-M_{EA9}. OTA operates at minimum voltage. The use of M_{EA7} and M_{EA9} reduces the size of MP power transistor which reduces area and gate capacitance. The Power MOS Mp is used because of its low voltage and low dropout voltage requirements. The gain provided by EA is low for fast transient response so current splitting technique is used in which gain is increase by using sufficient g_{m2} and increasing r_{09} which also increase PSR. First stage of the EA also contains M_{ta1}-M_{ta8} which reduces the Slew time of power MOS gate terminal.

![Schematic of proposed LDO](image)

**Fig. 1: Schematic of proposed LDO**

A. Steps to Design LDO (Methodology):

1) Schematic design of proposed LDO using CMOS transistors.
2) Determine different parameter mentioned above.
3) CMOS layout for the proposed LDO using VLSI backend tool
4) Verification of CMOS layout and parameter testing.
5) If detail verification of parameters is not done then again follow the first step with different methodology.

To realize the low drop out regulator, different methodology and techniques can be used. Considering the development of future technology and the advantage of 45nm technologies over 90 and 65nm technology, the proposed project has been decided to do with the selection of lower order of nm technology. Considering all these constraints regarding the demand of today’s fast communication and mobile world, the research has been undertaken to design low power low drop-out chip area efficient voltage regulator using 45nm CMOS technology. The proposed LDO is designed using 45 nm CMOS/VLSI technology in Advance Design System (ADS) Tool. As compared to 65nm/90nm CMOS technology, 45 nm CMOS technology offers:
- 30% increases in switching performance
- 30 % reduction in Power consumption
- 2 times higher density
- 2 times reduction of the leakage between source and drain and through the gate oxide.

Considering the advantages of 45 nm technologies over 90 nm & 65 nm technologies, the proposed work of designing low drop-out voltage regulator is done with 45 nm CMOS technology.

IV. EXPERIMENTAL RESULT

The proposed LDO is designed in 45 nm CMOS process. The LDO is capable of operating 1V, which covers a wide range of the typical battery voltage. The proposed LDO provides dropout voltage near about 200mV which is shown in below fig2.
V. CONCLUSION

The Proposed LDO is suitable for power management. This paper demonstrates new LDO design by considering exiting technologies; meeting today’s and tomorrow market demand. The circuit level implementation of proposed LDO carried out in Advance Design System (ADS). The LDO is design in 45nm CMOS process. The proposed LDO provides output voltage near about 0.8V from a 1V supply, and dropout voltage near about 200mV using a reference voltage of 0.4V. The LDO can be design by using different topologies and decreases dropout by 200 mV.

REFERENCES