Design of Rail-to-Rail Op-Amp in 90nm Technology

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Abstract

The output swing, dynamic range and the input common mode range of an operational amplifier are critical parameters of its performance in high power applications such as Bandgap reference circuits. It has been observed that these parameters reduce with advanced technology nodes and with lower supply voltages. With special biasing circuit, it is possible to raise the output swing and also common mode voltage. This paper presents a two stage, Rail to rail Operational Amplifier with Miller compensation and biasing circuit with a supply voltage of 1.2V in 90 nm CMOS technology. The design was carried out keeping in view the requirement of a Bandgap reference with a temperature coefficient of 1.34 ppm. The proposed design achieves a swing of 1.2V with a gain of 14 and UGB of 787 MHz. The physical design was carried out using Virtuoso tools for Custom IC design and physical verification with Assura toolset from Cadence®

Keywords: Bias generation, Class AB amplifier, Current Summing Circuit, Op-amp, Rail-to-Rail.

I. INTRODUCTION

An operational amplifier (op-amp) is a high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. An op-amp produces an output voltage that is typically hundreds of thousands of times larger than the voltage *difference* between its input terminals. Op-amp are characterised which is set by external components with little dependence on temperature changes or manufacturing variations in the op-amp itself, which makes op-amps popular building blocks for circuit design.

An Op Amp is a basic block in analog and mixed signal processing circuits, such as A/D, D/A circuits, switched-capacitor circuits and filters. With the reduction of the supply voltage, the performance of CMOS analog building blocks is degraded. The operation of the input stage is specially limited by the supply voltage. Thus, circuit design techniques to regain operating range and maintain good performance must be developed. For low-voltage Op Amp, a rail-to-rail operation is considered to keep a wide input signal range and good signal-to-noise ratio (SNR). The simple rail-to-rail input stage has an n-channel differential pair and a p-channel differential pair are connected in parallel as shown in figure 1. The total transconductance gm is halved at the ends of positive and negative input rails. To reduce signal distortion and maintain high performance, it is necessary to keep constant gm over the entire rails.

An operational amplifier (op-amp) is a high-gain differential stage with single-ended output or differential output. Many topologies of op-amps have been proposed in literature, both as general purpose and special purpose which are meant for specific applications. Generally, mixed signal design requires high gain, high settling time and low offset operational amplifiers. Communication applications such as filters and oscillators require wider bandwidth and high gain op-amps with good stability.

Power circuits such as voltage regulators and bandgap reference circuits, require moderate gain and high input common mode range and preferably rail to rail output swing op-amps. Operational Amplifiers such as Folded cascade topology in CMOS technology suffer from reduced output swing. Two stage operation was suggested in order to build up the output swing. Increase in gain is apparent in such designs with high power dissipation. Thus, circuit design techniques to regain operating range and maintain good performance must be developed. For low-voltage Op Amp, a rail-to-rail operation is considered to keep a wide input signal range and good signal-to-noise ratio (SNR).

The simple rail-to-rail input stage has an n-channel differential pair and a p-channel differential pair are connected in parallel as shown in Figure 1. The total transconductance g_m is halved at the ends of positive and negative input rails. Such a design requires constant g_m over entire range spanning the supply rails. This also reduces signal distortion and maintains high performance. Op-amps designed with NMOS input transistors, the input range is restricted near the negative power supply voltage. If the amplifier is designed with only PMOS transistors, the output can go beyond V_{DD}. If an amplifier uses both PMOS & NMOS transistors, it effectively combines the advantages of both types of transistors for true rail-to-rail input operation. When the input terminals of the amplifier are driven towards the negative rail the PMOS transistors are turned completely on and NMOS transistors are turned completely off and vice versa [1].

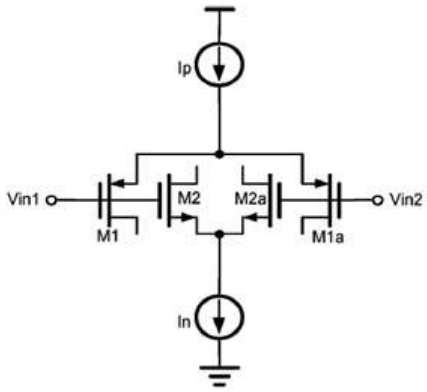

Figure 1 : Simple rail-to-rail input stage [1]

The rail-to-rail op-amp is used to compensate and maintain constant g_m over entire rails. However, the g_m of the n-channel input and that of the p-channel pairs is matched to obtain constant g_m. A rail-to-rail input stage with gm matching is applied in my work. A class-AB output stage is used to improve power efficiency and faster response.

II. ARCHITECTURE OF RAIL-TO-RAIL OP-AMP

Figure 2 shows the block diagram of the proposed rail-to-rail op-amp architecture. The architecture is composed of a bias circuit, a constant-g_m rail-to-rail input stage, a current summing circuit, and a class-AB output stage. The bias circuit provides the current sinks and the current sources. The input stage keeps constant total g_m over entire input common-mode range and maintains less signal distortion. The current summing circuit is used to sum the input currents and convert current gain into voltage gain. The class-AB output stage with high driving capacity can obtain wide swing.

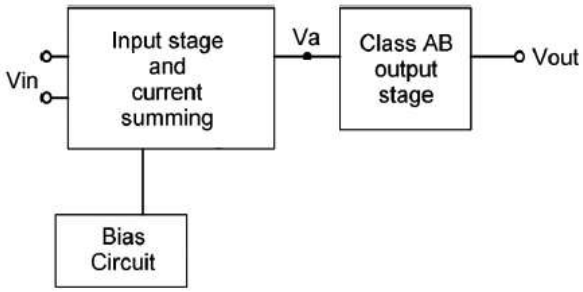

Figure 2 : Block diagram of rail-to-rail op-amp [1]

The input voltage range of the operational amplifier must be much larger than that to maintain the negative feedback of the circuit. The circuit of the rail-to-rail operational amplifier is illustrated in Figure 3. The input stage of the operational amplifier is consisted of pMOS transistor M1–M3 and nMOS transistors M11–M13, which will work alternatively in the lower and higher voltage range. Transistors M18–M19 forms the output stage of the rail-to-rail operational amplifier. The resistor *R* and capacitor *C* are used to compensate the right half plane zero to achieve enough phase margins. The bias current of the rail-to-rail operational amplifier is mirrored by transistor M20–M22. The current will compensate the decrease of the trans-conductance of the input stage with temperature. As a result, relatively stable dc gain is achieved over large operating point.

The current summing circuit is used to sum the p-channel and n-channel input current and to transfer the input stage total current to voltage. The cascode structure obtains high voltage gain due to its high output resistance. However, the bandwidth is degraded as the output load increases. The second stage is used to prevent the bandwidth degradation. By changing the current through current summing circuit, the slew rate can be improved. A zero is obtained using the compensation capacitor and resistor. The stability of the Op Amp can be improved by increasing the capacitance value. However, the bandwidth is sacrificed and the slew rate is degraded. A class-AB output stage provides a low output resistance and high power efficiency. Therefore, the bandwidth is not degraded at large output load.

The purpose of the class AB control circuit is to prevent the output transistors or any other transistors in the circuit from switching off, as this would deteriorate the step response of the stage. If the drain current of the n-channel output transistor (I_n) becomes very large the current through the p-type output transistor (I_p) has to be limited to a minimum value (I_{min}) and vice versa.

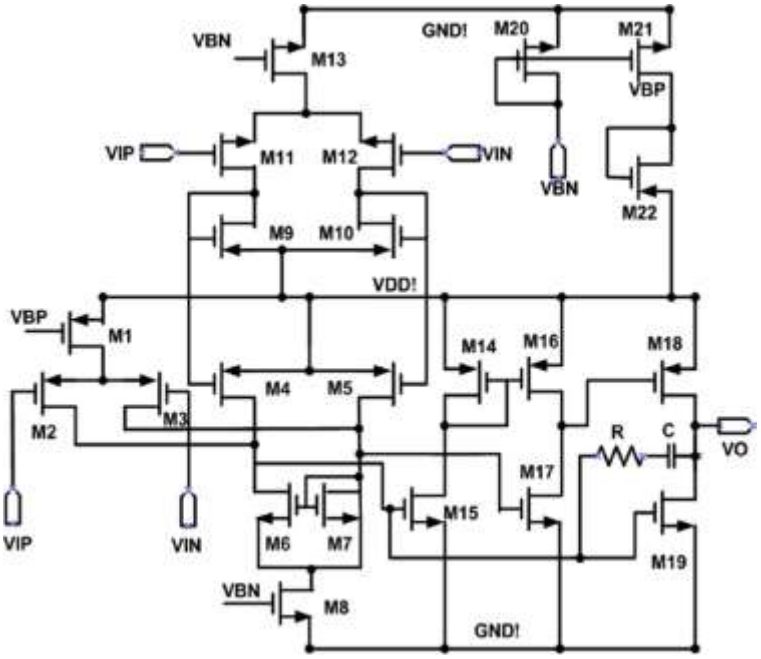

Figure 3 : Rail-to-rail operational amplifier [2]

Figure 4 shows the PMOS differential pair schematic diagram of the designed rail-to-rail op-amp in CADENCE environment. Figure 5 shows the class AB amplifier schematic of the rail-to-rail op-amp. Figure 6 shows the NMOS differential pair in rail-to-rail op-amp.

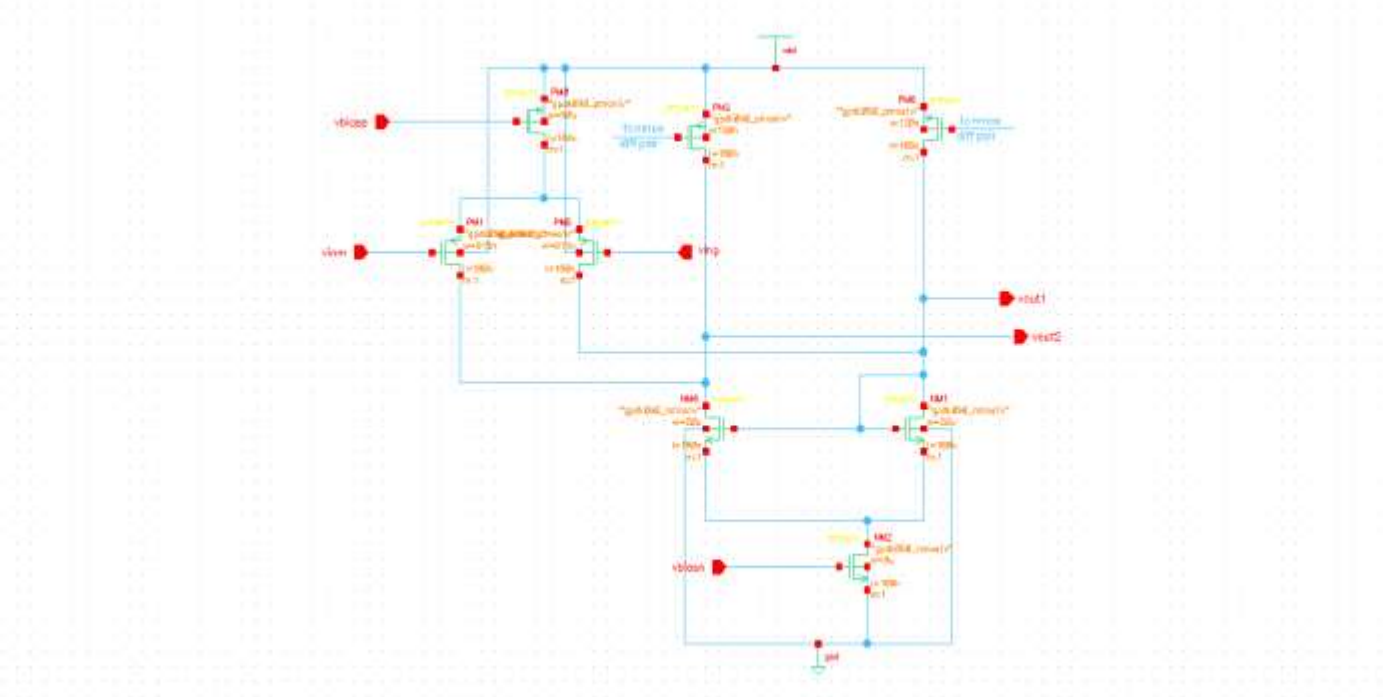

Figure 4 : PMOS differential pair schematic

Slew rate $SR = \frac{I5}{Cc}$(Assuming $I7 >> I5$ and $CL > Cc$) (1)

First-stage gain $A_{v1} = \frac{gm1}{gds2+gds4} = \frac{2gm1}{I5(\omega 2+ \omega 4)}$ where $\omega \rightarrow body\ effect$ (2)

Second-stage gain $A_{v2} = \frac{gm6}{gds6 + gds7} = \frac{gm6}{I6(\omega 6+ \omega 7)}$ (3)

Gain-bandwidth $GB = \frac{gm1}{Cc}$ (4)

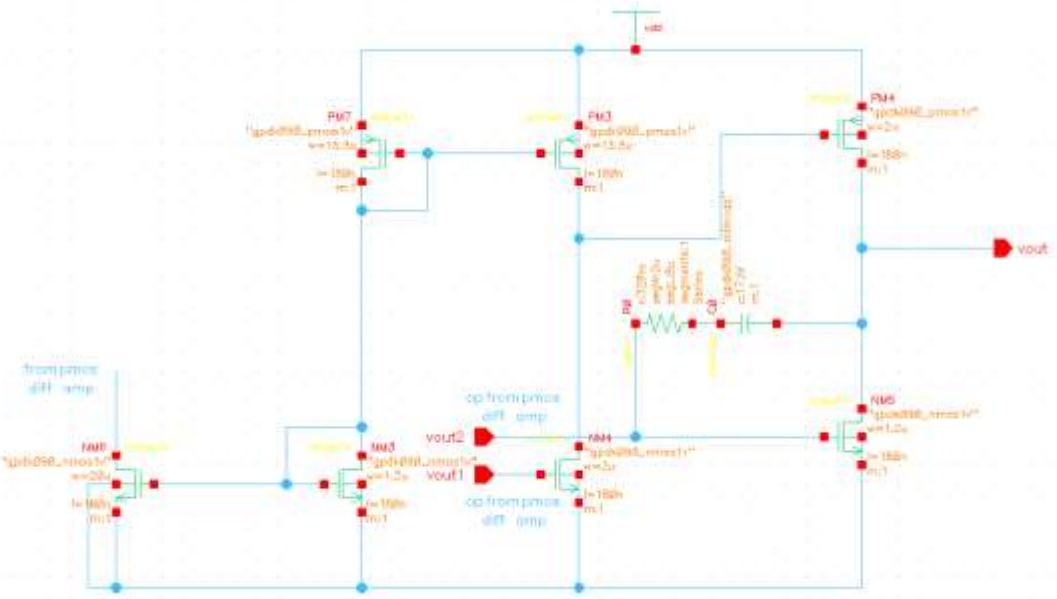

Figure 5 : Class AB amplifier schematic

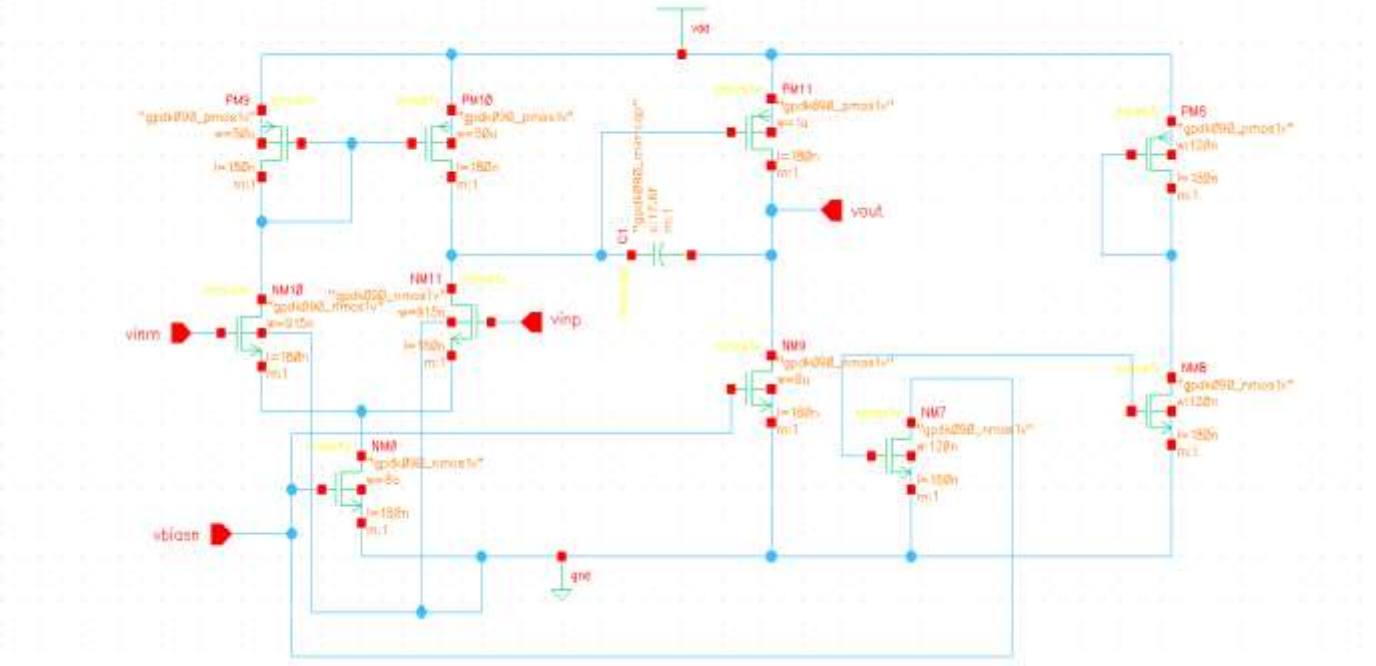

Figure 6 : NMOS differential pair schematic

$$\frac{vout}{vin} = \frac{gm1\ gm7\ R1\ R2\ (1-\frac{sCc}{gm7})}{1+sa+s2b} \qquad (5)$$

III. SIMULATION ENVIRONMENT

The design entry of the circuits is carried out in the CADENCE Analog Virtuoso Environment using gpdk90 library. For performance analysis these circuits are simulated in the Spectre simulator of CADENCE tool. Different characterstics of op-amp such as gain margin, phase margin, slew rate and settling time are measured in this environment. The AC and DC responses of the design is shown in Figure 7.

Output swing of the design is shown in Figure 8. Phase response of the design is shown in Figure 9. Settling time graph of the design is shown in Figure 10. Physical Layout has been done in the tool for the op-amp design and it is shown in the Figure 9.

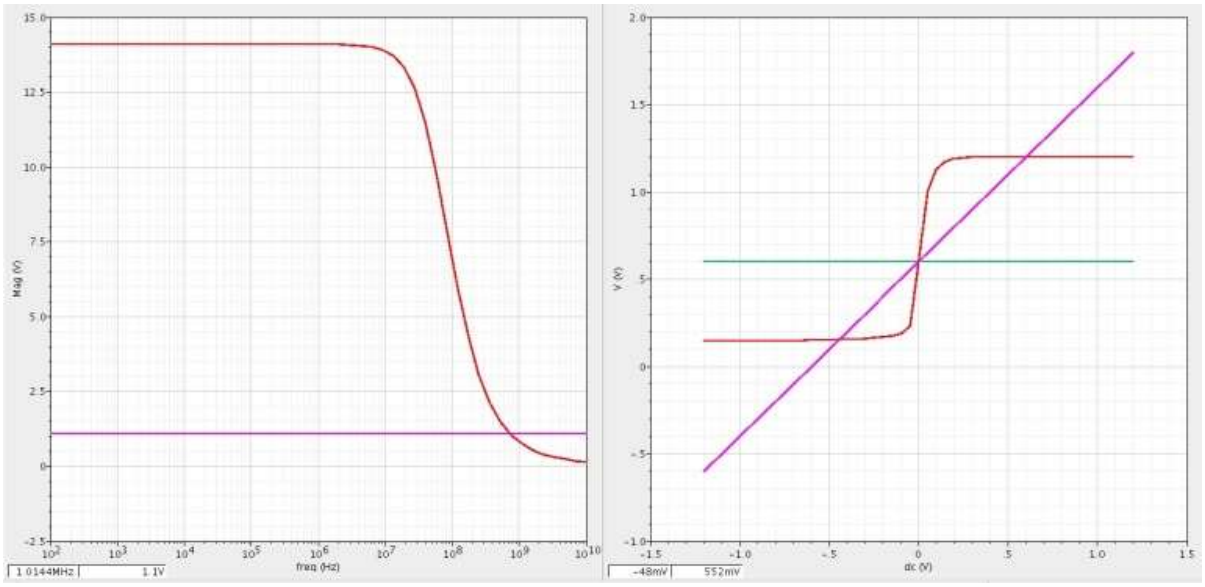

Figure 7 : AC and DC response of the design

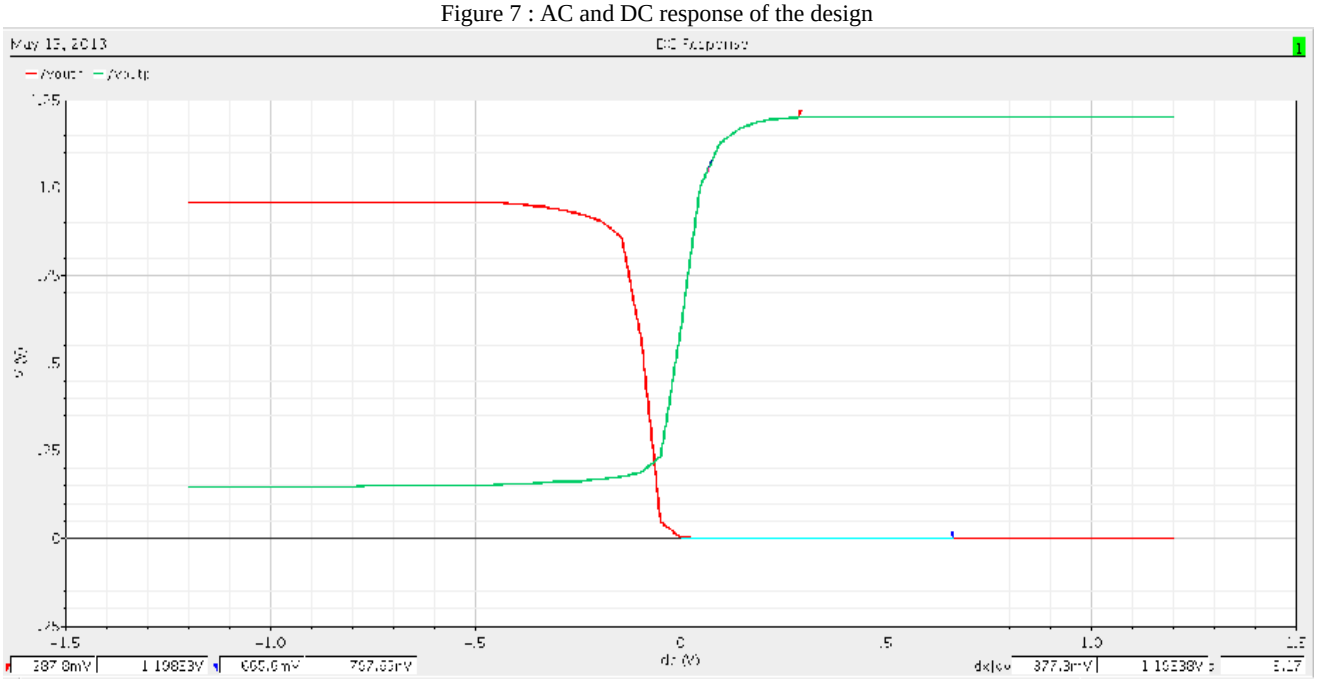

Figure 8 : Output swing

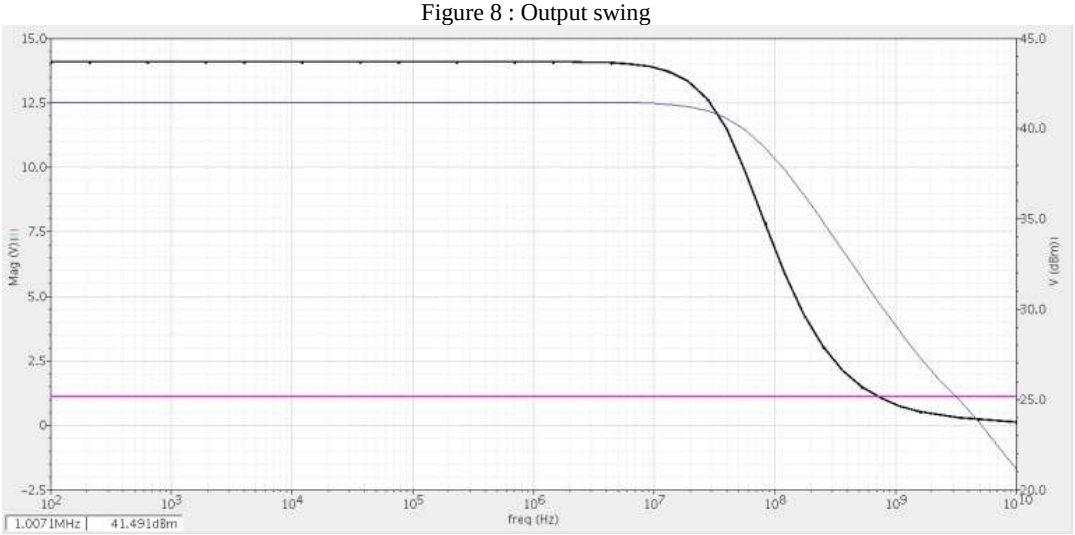

Figure 9 : Phase response of the design

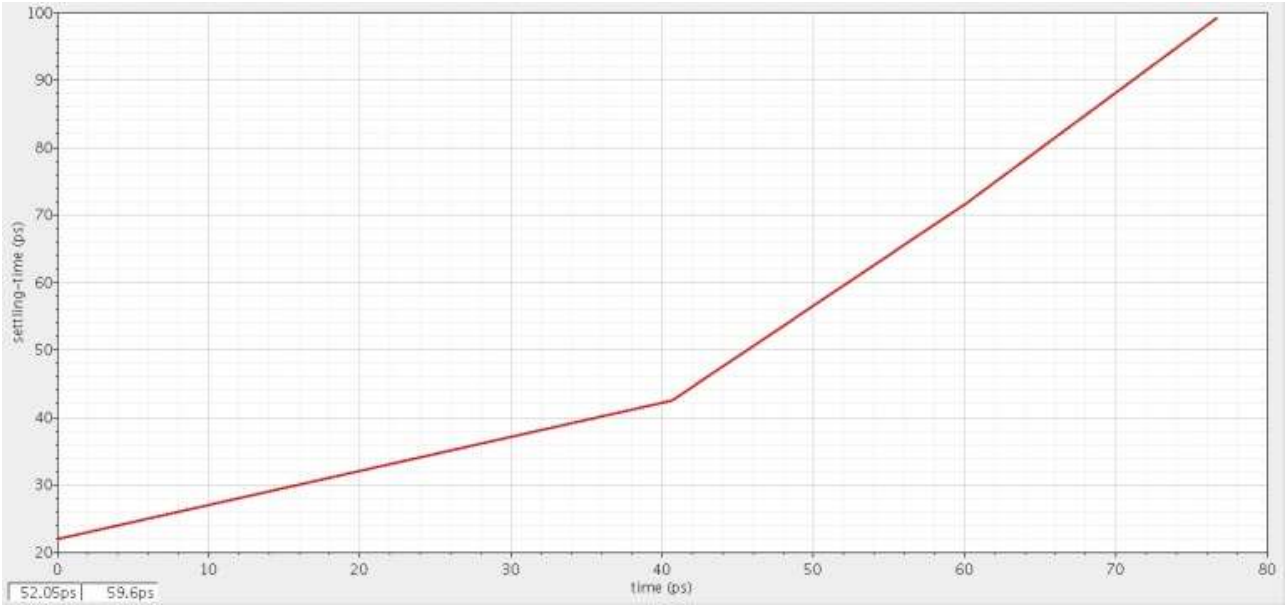

Figure 10 : Settling time graph of the design

IV. RESULTS

The rail-to-rail op-amp is designed for bandgap reference voltage generation circuit hence we have designed the circuit for gain of 14.

Table 1 : Performance summary

Parameter	***Value***
Supply Voltage	*1.2 V*
Gain	*14*
Unity Gain Frequency	*811.2MHz*
Gain Bandwidth Product	*787MHz*
Gain Margin	*-13.75*
Phase Margin	97.95^0
Slew Rate	*6.73V/us*
Settling Time	*2.066ps*
Rise Time	*935.8fs*
Fall Time	*926.6fs*

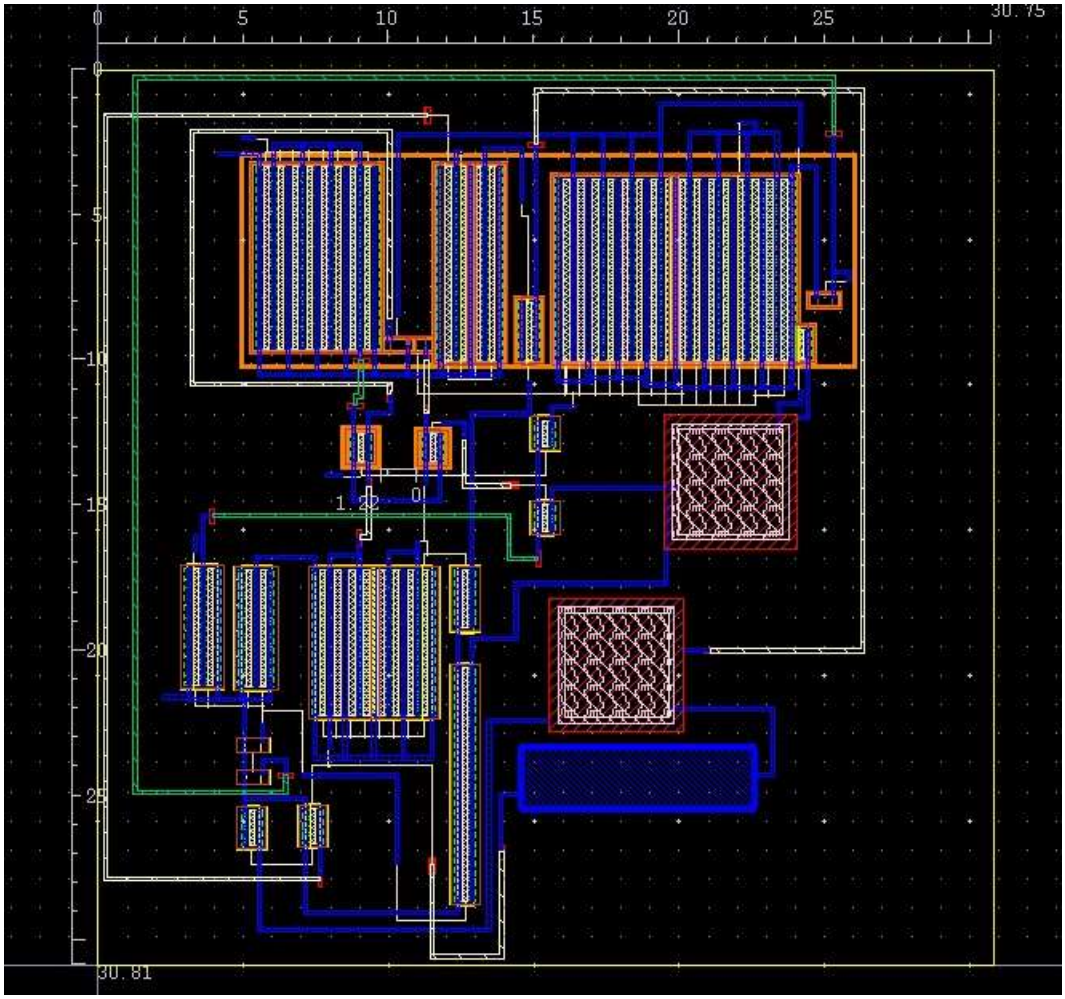

Figure 11 : Physical layout of rail-to-rail op-amp

V. CONCLUSION

A Rail-to-Rail input and output operational amplifier has been successfully designed in both schematic and layout. Physical design results match closely the design specifications. The performance including distortion of the op-amp is comparable to the same op-amp with a non Rail-to-Rail input stage I virtual earth configuration.

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