Piecewise Curvature-Corrected Bandgap Reference in 90 nm CMOS

P R Pournima
M.Tech
Electronics & Communication Engineering
B N M Institute of Technology, Bangalore, India

Abstract

A piecewise curvature-corrected CMOS bandgap reference (BGR) is proposed. It features in utilizing piecewise nonlinear curvature-corrected current and rail-to-rail operational amplifier to a conventional first-order current-mode BGR. The corrected current is zero, exponential with temperature and proportional to the squared temperature in the lower, middle and higher temperature range (TR). The rail-to-rail operational amplifier biased by a current proportional to absolute temperature (PTAT) helps to provide negative feedback for the proposed BGR. Measured results indicate that the proposed BGR achieves temperature coefficient (TC) of 3.72 ppm/ ^{0}C in the TR of -75 ^{0}C to +150 ^{0}C without trimming, power supply rejection (PSR) of -58 dB and line regulation of 2.4 mV/V in the voltage supply of 1.2 V. It is fabricated in 90 nm CMOS process with power consumption of 36 uW and effective chip area of 0.2 mm^2 . The physical design was carried out using Virtuoso tools for Custom IC design and physical verification with Assura toolset from Cadence®.

Keywords: Bandgap reference (BGR), Curvature-correction, Piecewise nonlinear, Power Supply Rejection(PSR), Rail-to-Rail, Temperature Coefficient (TC).

I. INTRODUCTION

Voltage reference is an essential block in most analog and mixed-signal applications, such as regulators, data converters, PWM controllers, oscillators, operational amplifiers, linear regulators and PLLs which are widely used in instrumentation and measurement systems. The resolution of precision ADCs is limited by the precision of its reference voltage over the supply voltage and operating temperate range. The bandgap reference (BGR) inherently exhibits low temperature coefficient (TC) and high power supply rejection (PSR), is the most popular voltage reference in integrated circuit. Bandgap voltage references typically provide a voltage around 1.2 V.

Some BGRs with low supply voltage are reported by using low threshold (or native) device[1], [2], Bipolar process[3], BiCMOS process[4], or Dual-Threshold MOS (DTMOS) process[5], which are either expensive or difficult to be integrated with digital system. This has resulted in the development of CMOS curvature-corrected BGRs in low supply voltage, such as piecewise- linear[6] and piecewise nonlinear curvature correction[7], temperature- dependent resistor ratio[8], current subtraction of two BGRs[9]. Standard CMOS process uses parasitic transistors and easily integrates with system implementation.

Temperature dependent drift of the reference voltage is undoubtedly one of the key issues in BGR design. It is known that the base-emitter voltage of the bipolar transistor is better characterized over temperature and varies less than the threshold voltage and mobility of the MOS transistors. Thus, most of the voltage references use the bipolar transistor's pn-junction as the basis of reference generation.

The performance of designs, which use a linear combination of a base-emitter voltage and a thermal voltage (BJT), is limited by the nonlinear dependence of the base emitter voltage. In order to achieve higher performance, several curvature compensation techniques were developed in which this is also one of the type. These techniques focus on cancelling the nonlinear dependence of base emitter voltage to some degree. In the piecewise linear method a nonlinear component is integrated at the output of a first order BGR in order to compensate its nonlinear behavior. In the different-type-resistor method different types of resistors are incorporated in the design in order to be able to cancel-out different orders of nonlinearity, thus achieving higher order correction. In this paper, we propose an alternative implementation which achieves a higher order cancellation for the base-emitter nonlinearity over a much wider temperature range. Proposed architecture uses two rail-to-rail op-amps, of which one is used in **PTAT** (**P**roportional **T**o **A**bsolute **T**emperature) and second op-amp is used to generate a **CTAT** (**C**omplementary **T**o **A**bsolute **T**emperature) current. This current is subsequently used to fine-tune the curvature correction mechanism so as to achieve a new level of performance. The proposed topology is sensitive to device mismatch, therefore resistor trimming is necessary to compensate for mismatch.

II. OPERATION OF CURVATURE CORRECTED BGR

The principal operation of first-order BGR is shown in Figure 1(a), the output voltage of which is given as

$$V_{ref} = K_1 V_{PTAT} + K_2 V_{BE} \quad (1)$$

where V_{PTAT} is a voltage proportional to absolute temperature (PTAT), K_1 and K_2 are temperature independent coefficients. V_{BE} is the base-emitter voltage of a bipolar transistor.

Considering the first-order temperature dependence, the base-emitter voltage is complementary to absolute temperature (CTAT), as shown in dashed line in Figure 1(a). The PTAT voltage compensates first-order temperature coefficient of V_{BE} by adjusting the coefficients of K_1 and K_2 to achieve a first-order BGR. But the minimum temperature coefficient of first-order BGR is nearly 20 ppm/^{0}C. To achieve lower temperature coefficient, curvature corrected BGR is necessary.

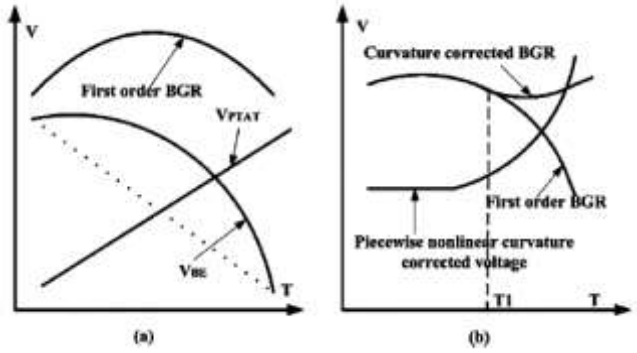

Fig. 1 : Curvature correction in BGR [10]

The operation of the proposed piecewise nonlinear BGR is shown in Figure 1(b). Here we choose the coefficient K_1 is slightly less than the calculated one in (1) to get a first-order BGR with negative temperature coefficient in the whole temperature range. But when the temperature is lower than T1, a lower temperature coefficient BGR in small temperature range is achieved. A piecewise nonlinear curvature-corrected voltage is added to the first-order BGR. When temperature is equal to T1, the piecewise nonlinear corrected voltage is zero. When temperature is higher than T1, a corrected voltage with higher temperature coefficient is generated, which will compensate the nonlinear temperature dependence of the first-order BGR shown in Figure 1(b). A piecewise nonlinear curvature-corrected BGR with lower temperature coefficient in larger temperature range is achieved.

III. CIRCUIT IMPLEMENTATION OF THE PROPOSED CURVATURE-CORRECTED BGR

The proposed nonlinear curvature-corrected BGR shown in Figure 2 consists of a startup circuit, a conventional first-order BGR and the proposed curvature- corrected current generator. The startup circuit formed by M1–M3 will work to avoid the undesired "zero" current state when the power supply is provided, which will not interfere with the normal operation of the BGR after the power supply is provided. The first-order BGR generate a reference with slightly negative temperature coefficient as shown in Figure 1(b). The curvature-corrected current generator generate a piecewise nonlinear current to corrected the nonlinear temperature dependence to achieve lower TC in larger TR.

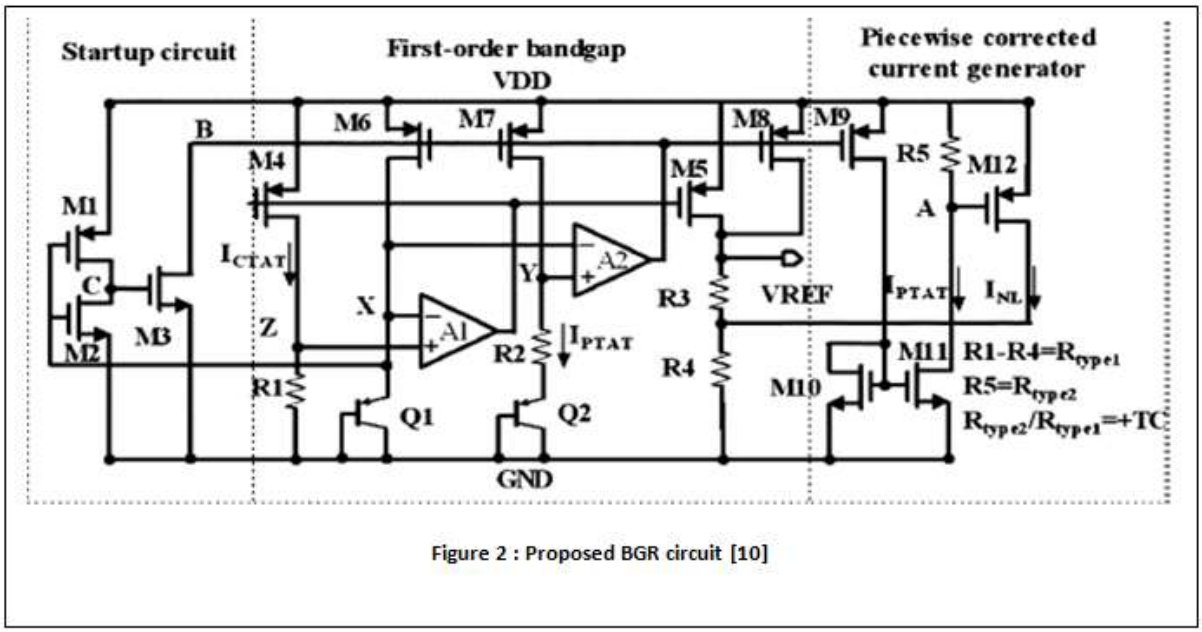

Figure 2 : Proposed BGR circuit [10]

A. Rail-to-Rail Operational Amplifier

Bias generation circuit is obtained by generating current reference. The bias voltage obtained by bias generation circuit is given to rail-to-rail op-amp, in order to bias the circuit. In the TR of -75 ^{0}C to 150 ^{0}C, the voltage of node X, Y, and Z will vary from 0.1 V to nearly 0.3 V. input voltage range of the operational amplifier must be much larger than that to maintain the negative feedback. While the threshold of nMOS and pMOS transistors are V_{Thn}=0.16 V and V_{Thp}=-0.13 V, respectively. Two rail-to-rail operational amplifiers are designed. The circuit of the rail-to-rail operational amplifier is illustrated in Figure 3.

The input stage of the operational amplifier is consisted of PMOS transistor M1–M3 and NMOS transistors M11–M13, which works alternatively in the lower and higher voltage range. Transistors M18–M19 forms the output stage of the rail-to-rail operational amplifier. The resistor *R* and capacitor *C* are used to compensate the right half plane zero to achieve enough phase margins. The bias current of the rail-to-rail operational amplifier is PTAT current with its static value of 2 uA, which are mirrored by the transistor M20–M22. The PTAT current will compensate the decrease of the trans-conductance of the input stage with temperature. As a result, relatively stable dc gain is achieved in larger temperature range.

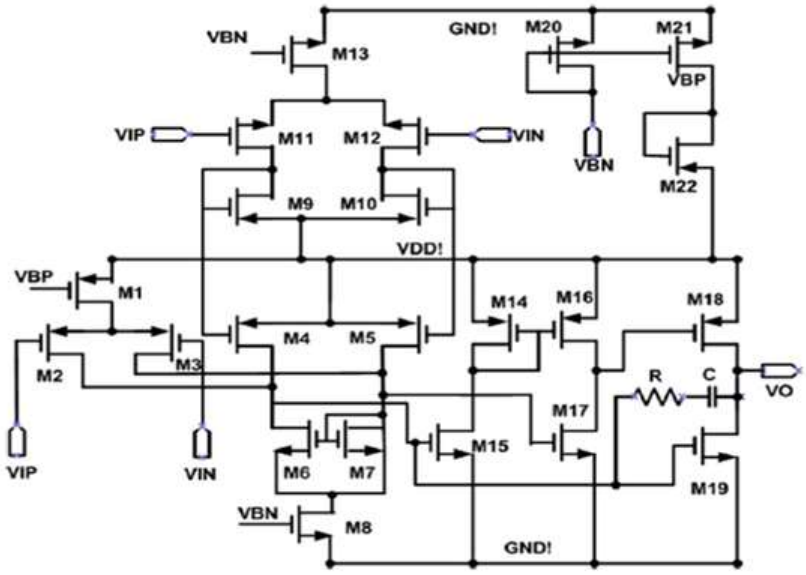

Fig. 2 : Rail-to-Rail op-amp schematic [10]

B. First-Order Current-Mode BGR

The schematic of the first-order current-mode BGR is shown in the middle of Figure 2. The operational amplifiers A1 and A2 are connected into negative feedback to ensure the node voltage at "X", "Y " and "Z" are the same with each other. As a result, a PTAT current and a first order CTAT current runs through transistor M7 and M4 respectively, which are mirrored and added to form a first-order current-mode BGR. The output voltage of the first-order BGR is also expressed as

$$V_{ref} = K_3 \times V_{G0} + \frac{KT}{q}(\eta - \alpha)\, ln\frac{T}{T_R} \qquad (2)$$

where the coefficient K_3 according to (2) is a coefficient independent of temperature with its value less than 1. The simulated TC of the first order BGR is about 3.72 ppm/ ^{0}C in the TR of -75 ^{0}C to +150 ^{0}C.

C. Proposed Curvature-Corrected Method

The operation of the proposed piecewise corrected current generator is graphically illustrated in Figure 4. It consists of PTAT current, resistor R5 and transistor M12. The temperature-dependent resistor ratio technique in [14] is utilized to achieve a PTAT voltage. As a result, the TC of R5 must be higher than that of R2. The voltage at node "A" is given as

$$V_A = V_{DD} - \frac{R_5 \times V_T \times \ln(n)}{R_2} \qquad (3)$$

Due to the positive TC of R5/R2, a PTAT voltage is achieved at the gate-source voltage of transistor M12,

$$V_{SG-M12} = \frac{R_5 \times V_T \times ln(n)}{R_2} \qquad (4)$$

When $V_{SG\text{-}M12}$ is much lower than its threshold voltage V_{Thp}, there will be no current through M12. When $V_{SG\text{-}M12}$ is closing and still lower than its threshold, M12 operates in weak inversion. When $V_{SG\text{-}M12}$ is higher than its threshold, M12 works in saturated region, I_{NL} is given as

$$I_{NL} = \frac{1}{2} \times u_p \times C_{OX} \times \frac{W}{L} \times (V_{SG-M12} - |V_{Thp}|)^2 \times (1 + \lambda V_{DS}) \qquad (5)$$

where u_p is the electron mobility, C_{OX} is the gate capacitance per unit area, λ is the Channel Length Modulation. The temperature dependence of electron mobility is approximately expressed as u_p is inversely proportional to T^2. Considering the higher-order temperature dependence and neglecting the lower one in (5), the approximate temperature dependence of I_{NL} to T^2 is achieved.

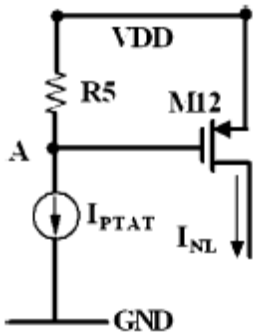

Fig. 3 : Piecewise linear curvature corrected current circuit [10]

The piecewise curvature-corrected current is outlined as

$$I_{NL} = \begin{cases} 0, & V_{SG\_M12} \ll |V_{Thp}| \\ \propto \exp(T), & V_{SG_{M12}} \leq |V_{Thp}| \\ \propto T^2, & V_{SG\_M12} > |V_{Thp}| \end{cases} \qquad (6)$$

When the temperature is less than 30 ^{0}C, the nonlinear corrected current is zero, which is the critical temperature of T1 in Figure 1(b). The nonlinear corrected current is exponential with temperature in the TR of 30 ^{0}C to 70 ^{0}C, proportional to squared temperature when the temperature is higher than 70 ^{0}C.

IV. CIRCUIT IMPLEMENTATION

The principle of the proposed BGR is to combine the piecewise nonlinear current I_{NL}, I_{PTAT} and I_{CTAT} to provide a curvature-corrected current, which is transferred into a curvature corrected voltage by a resistor. The PTAT current through M8 in the first-order BGR is mirrored by M9–M11 to form the PTAT current of Figure 4. The piecewise corrected current I_{NL} runs through R4 to generate the corrected voltage. The output voltage of the proposed BGR is the addition of the first-order current-mode BGR and the corrected voltage, which is

$$V_{ref} = \left(\frac{V_{BEQ1}}{R_1} + \frac{V_T \ln(n)}{R_2}\right) \times (R_3 + R_4) + I_{NL} \times R_4 \qquad (7)$$

The minimum supply voltage of the piecewise nonlinear current generator and that of the first-order BGR is $V_{SG\text{-}M10}+V_{DS(sat)}$ and $V_{BEQ1}+V_{DS(sat)}$ respectively. In a word, the minimum supply voltage requires for the proposed BGR is 1.2 V,

which is mainly limited by the threshold of the pMOS transistor. In this way a piecewise nonlinear curvature corrected BGR with low supply voltage is generated.

V. EXPERIMENT RESULT

The piecewise nonlinear curvature corrected BGR is designed and fabricated in 90 nm CMOS process technology. The resistors R1–R4 are designed of p^+ diffusion with temperature coefficient of 8.5e-4 Ω/ ^{0}C, while R5 is designed of n-well with temperature coefficient of 5.6e-3 Ω/ ^{0}C to generate the piecewise curvature-corrected current. The mismatch of the operational amplifier and that of resistor R1–R4 will decrease the achieved temperature coefficient dramatically. When placing the layout, great attention is paid to input transistors of the rail-to-rail operational amplifier, and resistors of R1–R4 are implemented by using the same resistor unit to minimize the mismatch.

Table 1 : Performance at different process corners

Library process corners	***V_{ref} at 25^0 C***	***Temperature Coefficient***
NN	*1.198*	*3.64 ppm/ ^{o}C*
SS	*1.198*	*5.42 ppm/ ^{o}C*
SF	*1.199*	*2.51 ppm/ ^{o}C*
FS	*1.197*	*6.24 ppm/ ^{o}C*
FF	*1.198*	*2.75 ppm/ ^{o}C*
NN high performance	*1.198*	*3.73 ppm/ ^{o}C*
SS high performance	*1.197*	*5.42 ppm/ ^{o}C*
SF high performance	*1.198*	*2.51 ppm/ ^{o}C*
FS high performance	*1.197*	*6.24 ppm/ ^{o}C*
FF high performance	*1.198*	*2.76 ppm/ ^{o}C*

The robust of the proposed BGR is verified by processing it in different process corners using corner simulation. The simulated result of process corner is shown in Table 1. As given in Table 1, the TR will be affected by resistor variation. But TC of 3.72 ppm/ ^{0}C in the TR of -75 ^{0}C to 150 ^{0}C is achieved in the worst case of process corner variation. As is shown in Table 1, the TC is slightly affected by process corners. But the minimum power supply varies dramatically with variation of transistor threshold, especially that of pMOS transistor. The reason for that is the threshold of PMOS transistor is much larger than that of NMOS transistor. The proposed BGR achieves TC of less than 6.24 ppm/ ^{0}C in the worst corner simulation.

Table 2 : Comparison between different Curvature Corrected BGR

Parameters	***This work***	***Ref [5]***	***Ref [6]***
Measured TC	*3.72 ppm/ ^{0}C*	*5.3 ppm/ ^{0} C*	*19.5ppm/ ^{0}C*
Temperature Range	*-75 to 150 ^{0}C*	*0 to 100 ^{0}C*	*0 to 100 ^{0}C*
Process	*90 nm CMOS*	*0.6um CMOS*	*0.25um CMOS*
Power	*36uW*	*46uW*	*50uW*
Supply Voltage	*1.2V*	*2V*	*1V*
PSRR	*-58dB*	*-47dB*	*-*
Line Regulation	*2.4mV/V*	*1.43m/V*	*-*

Table 2 lists performance comparison of some published state-of-art curvature-compensated BGRs with this work. The proposed BGR achieves lower TC in the TR of 225 ^{0}C, while the TR in [15] is only 100 ^{0}C. Comparison result shows lower TC in a larger TR is achieved by the proposed BGR. The minimum power supply of the proposed BGR is higher than that in [15], which is mainly limited by the threshold of the PMOS transistor of this process. The TC of the proposed BGR at 1.2 V supply voltage is in the almost same level with that of [14] with 2 V supply voltage.

VI. CONCLUSION

A piecewise nonlinear curvature-corrected CMOS BGR has been proposed. Temperature dependence of proposed BGR is measured with the operating temperature range varying from -75 ^{0}C to 150 ^{0}C. The measured temperature dependence will deteriorate when the supply voltage is lowered to less than 1.2V. The proposed BGR achieves TC of 3.72 ppm/ ^{0}C, PSR of -58 dB and line regulation of 2.4 mV/V at 1.2V supply. The maximum power consumption is 36 uW, among them 24 uW power consumption is dissipated by the two rail-to-rail operational amplifiers. Table 2 lists performance comparison of some published state-of-art curvature-compensated BGRs with this work. The proposed BGR achieves lower TC in the TR of 150 ^{0}C, while the TR in [15] is only 100 ^{0}C. Comparison result shows lower TC in a larger TR is achieved by the proposed BGR. The minimum power supply of the proposed BGR is higher than that in [15], which is mainly limited by the threshold of the PMOS transistor of this process. The TC of the proposed BGR at 1.2 V supply voltage is in the same level with that of [14] of 3.72 ppm/^{0}C.

Figure 5 shows the layout of complete BGR circuit which has an area of 0.2 mm^2. Figure 6 shows the output waveform of designed BGR circuit. Figure 7 shows the plot of V_{ref} Vs V_{DD} of proposed BGR circuit. Figure8 shows the plot of V_{ref} Vs Temperature of proposed BGR circuit.

Fig. 4 : Layout of BGR circuit

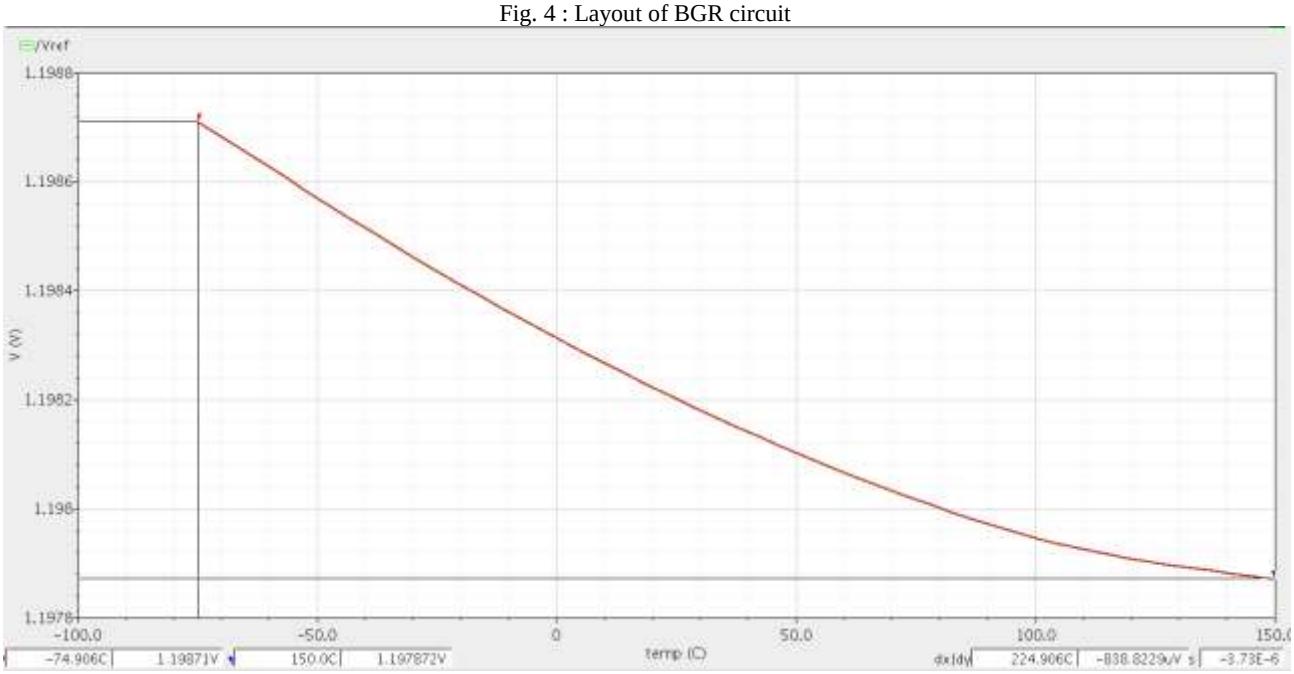

Fig. 5 : Proposed BGR circuit output

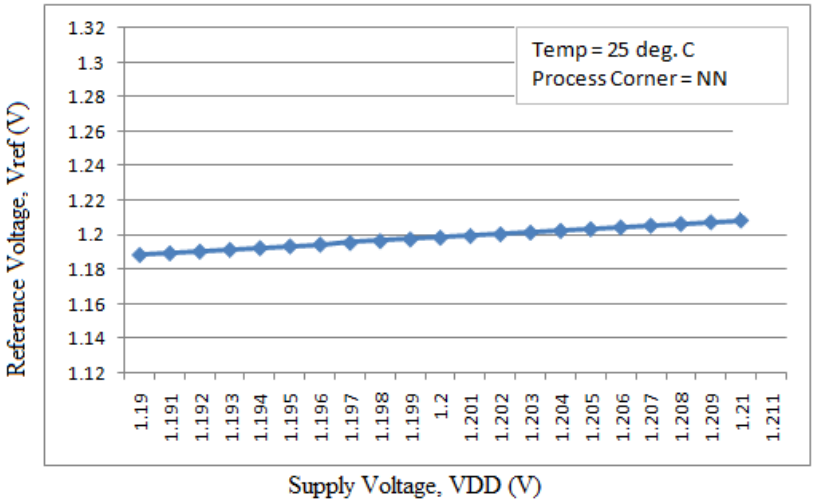

Fig. 6 : Plot of V_{ref} Vs. V_{DD} for proposed BGR circuit

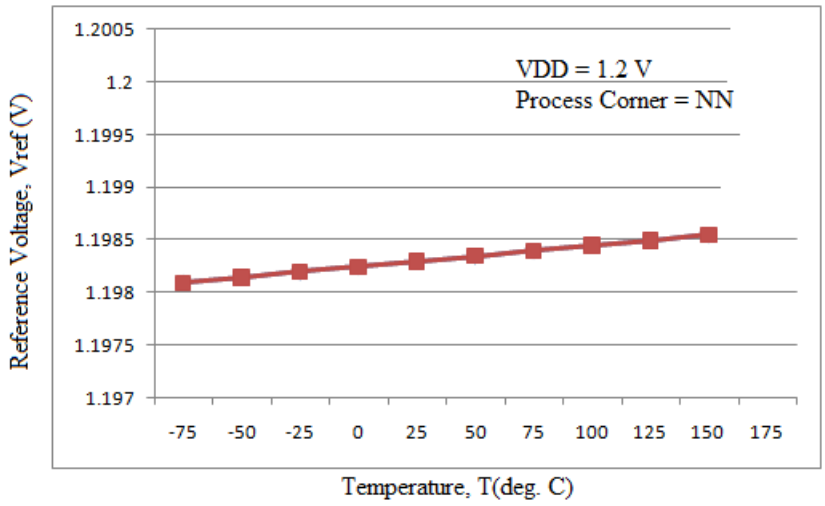

Fig. 7 : Plot of V_{ref} Vs. Temperature of proposed BGR circuit

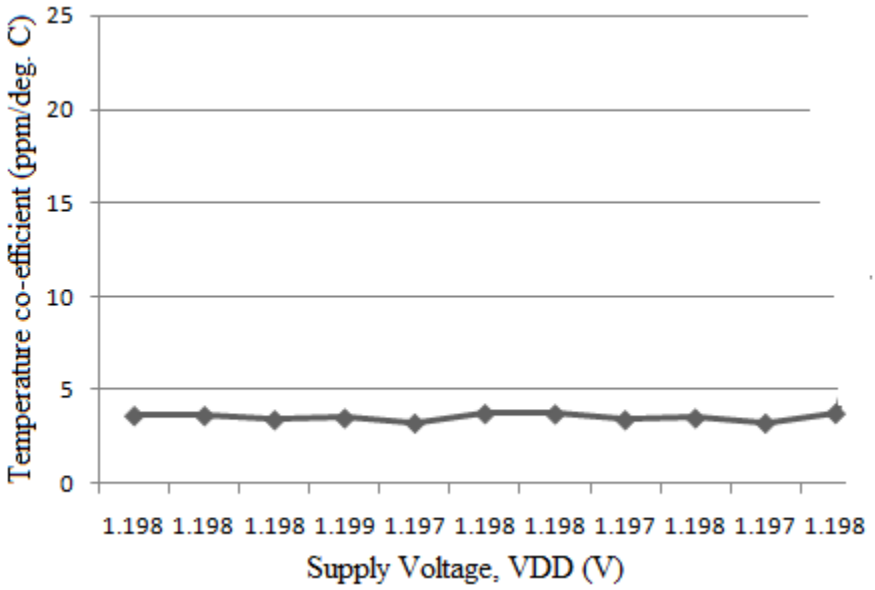

Fig. 8 : Measured temperature co-efficient of BGR circuit

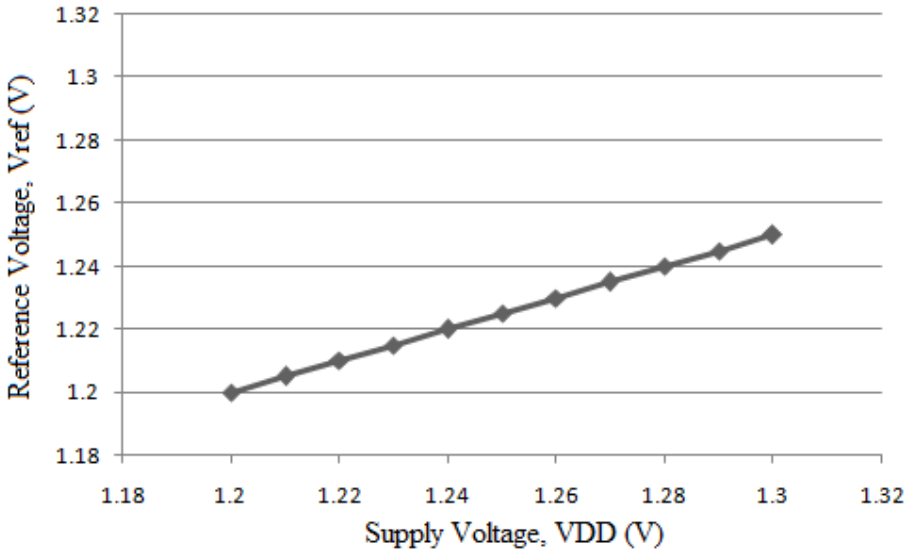

Fig. 9 : Measured line regulation at different loads

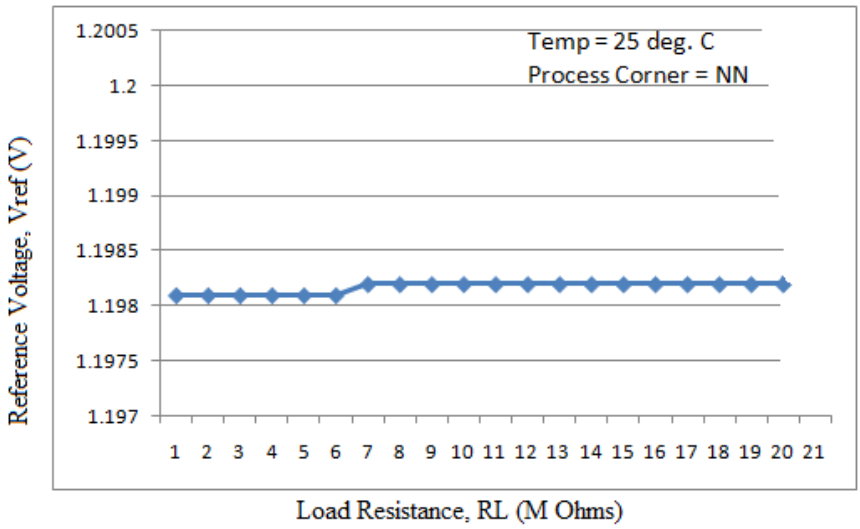

Fig. 10 : Plot of V_{ref} vs R_L (different loads) of proposed BGR circuit

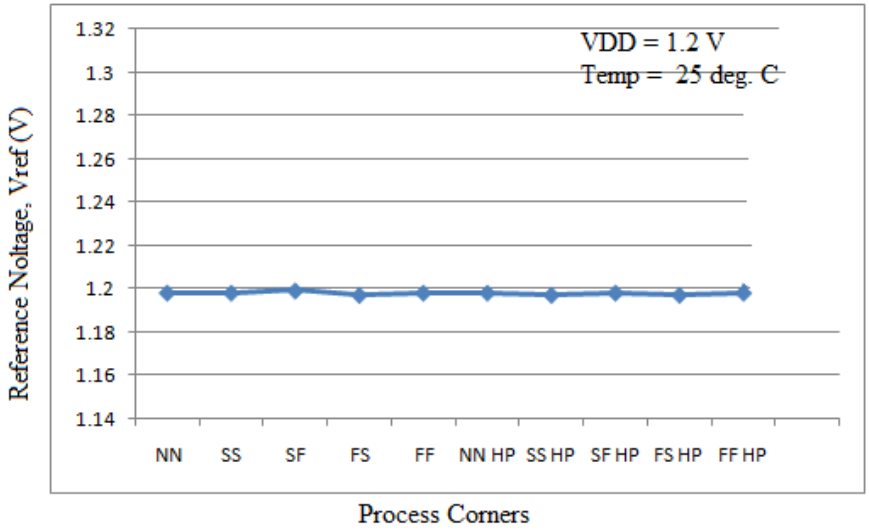

Fig. 11 : Plot of proposed BGR circuit output at different process corner

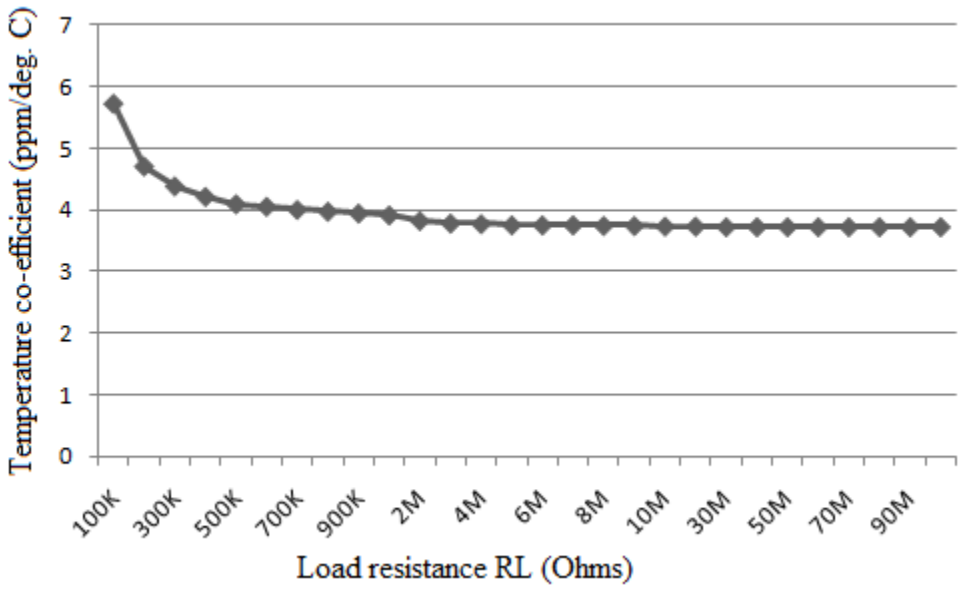

Fig. 12 : Measured load regulation of proposed BGR circuit

ACKNOWLEDGEMENT

This work has been supported by all the teaching staff and non-teaching staff of BNMIT, Bangalore. The author takes this opportunity to thank specially the internal guide for this project Mrs. P Prabhavathi, Associate Professor, BNMIT. The author also wish to thank the Management & Administration of BNMIT, Bangalore for the support and guidance in the bringing the paper successfully.

REFERENCES

[1] G. Giustolisi, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 151–154, Jan. 2003.
[2] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap voltage reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.
[3] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap reference," *IEEE J Solid-State Circuits*, vol. 28, no. 6, pp. 667–670, Jun. 1993.
[4] P. Malcovati, F. Maloberti, M. Pruzzi, and C. Fiocchi, "Curvature compensated BiCMOS bandgap with 1-V supply voltage," *IEEE J Solid- State Circuits*, vol. 36, no. 7, pp. 1078–1081, Jul. 2001.
[5] A.-J. Annema, "Low-power bandgap voltage references featuring DTMOSTs," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 949–955, Jul. 1999.
[6] G. A. Rincon-Mora and P. E. Allen, "A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1551–1554, Oct. 1998.
[7] J. H. Lee, Y. N. Fu, and Y. S. Wang, "A 1-V piecewise curvature-corrected CMOS bandgap reference," in *Proc. IEEE Int. Symp. Low Power Electron. Des.*, Bangalore, India, 2008, pp. 289–294.
[8] K. N. Leung and P. K. T. Mok, "A 2-V 23 uA 5.3 ppm/ curvature-compensated CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 561–564, Mar. 2003.
[9] M. D. Ker and J. S. Chen, "New curvature compensated technique for CMOS bandgap reference with sub-1-V operation," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 53, no. 8, pp. 667–671, Aug. 2006.
[10] Jing-Hu Li, Xing-bao Zhang, and Ming-yan Yu "1.2-V Piecewise Curvature-Corrected Bandgap Reference in 0.5 um CMOS Process." *IEEE transactions on Very Large Scale Integration (VLSI) systems*, vol. 19, no. 6, Jume 2011, pp. 1118-1122.
[11] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature- corrected low-voltage bandgap reference," *IEEE J Solid-State Circuits*, vol. 28, no. 6, pp. 667–670, Jun. 1993.
[12] B. S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 634–643, Jun. 1983.
[13] G. A. Rincon-Mora, *Voltage References from Diode to Precision High-Order Bandgap Circuits*. New York: Wiley, 2002, pp. 45–119.
[14] K. N. Leung and P. K. T. Mok, "A 2-V 23 uA 5.3 ppm/ curvature- compensated CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 561–564, Mar. 2003.
[15] M. D. Ker and J. S. Chen, "New curvature compensated technique for CMOS bandgap reference with sub-1-V operation," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 53, no. 8, pp. 667–671, Aug. 2006.