Verilog Modeling of Wi-Fi MAC Layer for Transmitter

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Abstract

The main objective is to design and implementation WIFI MAC Transmitter using Verilog.For the wireless communication in RF range IEEE 802.11 is one of the many standards available .IEEE 802.11b defines the Medium Access Control Layer for wire less local area networks. Wi-Fi MAC transmitter module is divided into 5 blocks I.e.. data unit interface block, controller block, payload data storage block, MAC header register block, data processing block.In this project, we are considering only two blocks i.e. payload data storage block, data processing block.

Keywords: Wi-Fi MAC layer, IEEE 802.11b, Header block, FPGA, Logic analyzer

I. INTRODUCTION TO WIFI

Wireless Technology is an alternative to Wired Technology, which is commonly used, for connecting devices in wireless mode.Wi-Fi (Wireless Fidelity) is a generic term that refers to the IEEE 802.11 communications standard for Wireless Local Area Networks (WLANs).Wi-Fi Network connect computers to each other, to the internet and to the wired network. The WLAN (Wireless Local Area Network) protocol, IEEE 802.11, allows wireless and mobile network access to a network infrastructure. Before the 802.11b protocol (which was coined Wi-Fi) was widely adopted in the early 2000s, to get high speed network access to your LAN you had to be physically connected via a cable. The family of 802.11 protocols are made up of an arrangement of over-the-air modulation techniques that use the same basic principles. The most widely used protocols are the 802.11b, 802.11g and 802.11n for 2.4GHz networks and the 802.11a, 802.11n and 802.11ac for 5GHz networks.

II. OVERVIEW OF MAC LAYER

Before transmitting frames, a station must first gain access to the medium, which is a radio channel that stations share. The 802.11 standard defines two forms of medium access, distributed coordination function (DCF) and point coordination function (PCF). DCF is mandatory and based on the CSMA/CA (carrier sense multiple access with collision avoidance) protocol. With DCF, 802.11 stations contend for access and attempt to send frames when there is no other station transmitting. If another station is sending a frame, stations are polite and wait until the channel is free.

As a condition to accessing the medium, the MAC Layer checks the value of its network allocation vector (NAV), which is a counter resident at each station that represents the amount of time that the previous frame needs to send its frame. The NAV must be zero before a station can attempt to send a frame. Prior to transmitting a frame, a station calculates the amount of time necessary to send the frame based on the frame's length and data rate. The station places a value representing this time in the duration field in the header of the frame. When stations receive the frame, they examine this duration field value and use it as the basis for setting their corresponding NAVs. This process reserves the medium for the sending station.

Medium Access control [MAC] layer performs function like i) On transmission, assemble data in to a frame with address and error detection fields ii) On reception, disassemble frame and perform address recognition and error detection iii) Govern access to the LAN transmission medium Physical layer performs| functions like. i) Encoding/decoding of signals ii) I Preamble generation/ removal [for Synchronization].iii) Bit transmission I reception iv) Includes specifications of the transmission medium [4].

III. WI-FI FEATURES

Wi-Fi Wireless Fidelity [802.11 family of standards] for LAN. WiFi is designed for local areanetworks, which are private, local (short range), but wherecompeting cable systems run at very high speeds. WiFi .achieves greater than lOMBit/ Sec throughput for a user in many circumstances. Currently WiFi carries more user data than any other wireless technology. Evolution is to go

further, faster and at lower power consumption [2] Upstart wireless LAN [WLAN] technologiesFunder the 802.11 (Wi-Fi) umbrella have leapfrogged Ktowards cellular and other efforts edging towards broad I0 band wireless [such as 802.16! WiMAX] and have led to Have the first wide spread, commercially successful broadband wireless access technology . Infact, Wi-Fi is a runaway A a success around the globe [5].

IV. PROPOSED BLOCK DIAGRAM OF TRANSMITTER

As discussed earlier, the transmitter block is Fig 4 Block diagram of transmitter divided in to five parts as shown in fig 4 and only two blocks are considered for VHDL simulation. These are Payload Data Storage block & Data Processing block

A. Payload Data storage block

Is further divided into two modules i.e. FIFO module & Data length counter module. These modules are discussed as shown below.

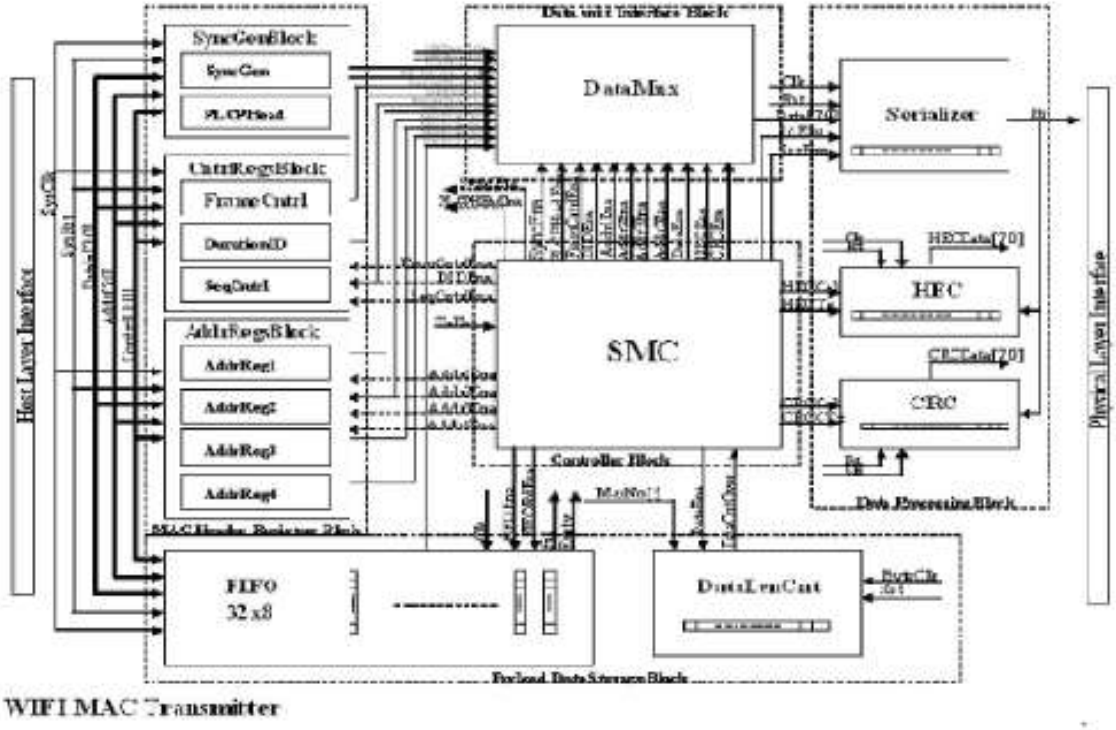

Fig. 1: Block Diagram Of Transmitter

1) *FIFO Module*

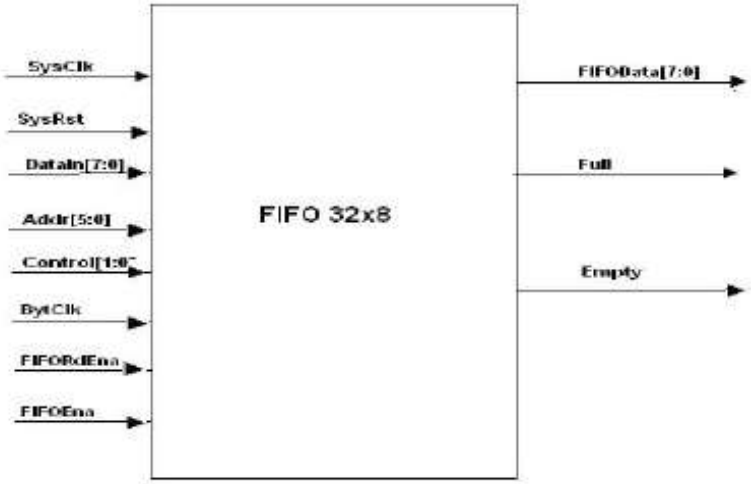

Fig. 4.1 a: FIFO Module

Description:
FIFO Module is shown in Figure 4.1 a. It contains the data to be transmitted. It acts as the synchronizing tool i.e. the data are entered at high rate but it is retrieved at the slower rate. Here, we have taken 32x8 bits of data storage. Here, the first incoming data goes out first.

It acts on two clocks i.e. SysClk and ByteClk, on their rising edge and when the FIFO is enabled the input data is retrieved. The Full and Empty signals shows the state of the FIFO.

2) *Data length counter module*

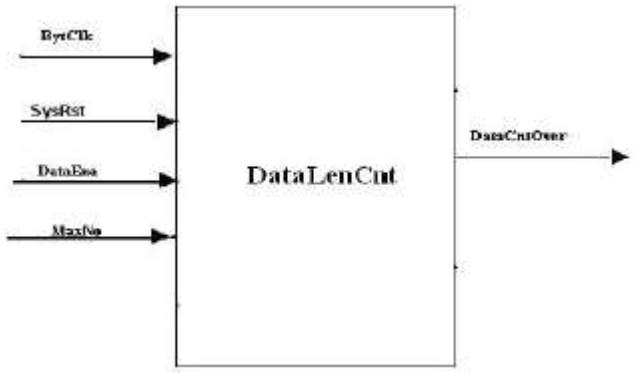

Fig. 4.1 b: Data length counter module

Description:
Fig. 4.1 b shows Data length conter module. This module acts as a counter. It simply accepts a Max Number and counts the data being transmitted. When the number field of the data is equal to the Max Number then the Data When the TxEna signal is high, then the CRC data is CountOver signal is turned high. It acts at every rising given out and when the CRCCIEna is high, then the CRC edge of the clock.

B. Data Processing Block
It is divided in to three modules i.e, serializer module,HEC and CRC modules and they are discussed in details as shown below

1) *SerialiZer Module*

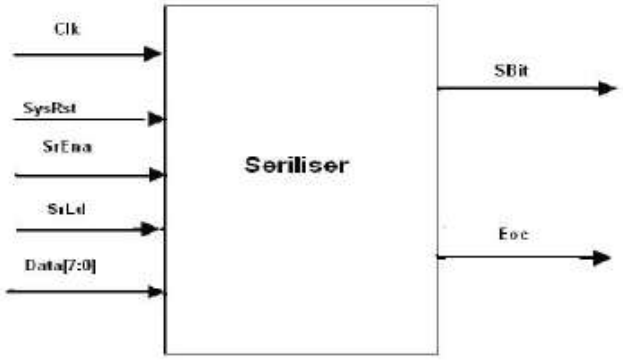

Fig.4.2(a): SerialiZer Module

Description:
Fig. 4.2 a shows serializer Module. It is basically the parallel input and serial out put device. Various data selected at the multiplexer are serially obtained. It occurs at every rising edge of the clock and when the serial enable is high. The output bit is designated as SBit. When all the output bits are over, then the End of Conversion i.e. efficiency of EOC goes high.

2) *HEC Module*

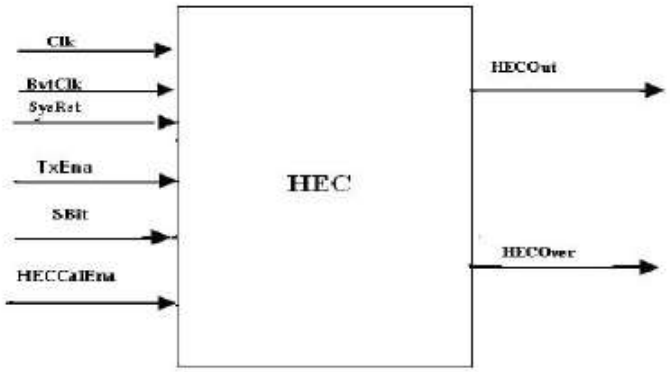

Fig 4.2b: HEC Module

Description:

Fig. 4.2 b shows HEC Module. This module produces the Head Error Check bits. It is the 16-bit error check bit. The HEC is calculated when the HRCCalEna is high and when the TxEna is high then the HEC data is transmitted along with the PLCP Header Bits.

3) *CRC Module*

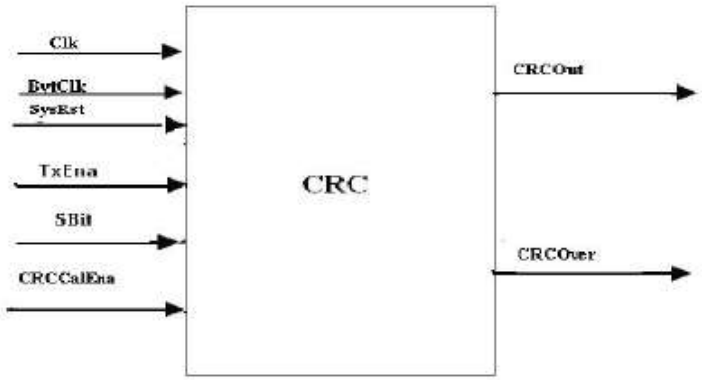

Fig 4.2c: CRC Module

Description:

4.2 c shows CRC Module. The CRC is 32 bit field containing the 32-bit Cyclic Redundancy Check.When the TxEna signal is high, then the CRC data is given out and when the CRCCIEna is high, then the CRC is calculated. CRCOver is high when the transmission of the data is over. This module helps in error free transmission of the data with proper reliability.

V. VERILOG MODELING OF WI-FI MAC LAYER FOR TRANSMITTER

There are two types of widely used hardware description languages i.e. Verilog HDL with C-language like syntax, easy to learn and another is VHDL which follows the structure of ADA programming language.Verilog and VHDL each have about 50% share of the commercial user base [8].

Due to high computational complexity of WLAN systems and the capabilities of state-of-the-art microprocessor s, an implementation based solely in microprocessors would require a large number of components and would be cost inefficient FPGAs with their spatial / parallel computation style can significantly accelerate complex parts of WLANs and improve the efficiency of discrete components implementations[I0].

The design has been synthesized using FPGA.This device belongs to the virtex -E group of FPGAs from xilinx. Two types of FPGAs (Field Programmable Logic Array) are available i.e.i) Reprogrammable (SRAM based) from Xilinx, Altera, Lattice and Atmel ii) Onetime Programmable (OTP) from Actel, Quick logic.

FPGAs are reasonably cheap, with short design cycle and are reprogrammable. They are more flexible than PLDs and more compact than MSI/SSI. FPGAs have evolved to meet new application demands with features like i) Newer devices incorporate entire CPUs i.e. Xilinx,Virtex II pro has 1-4 power PC CPUs ii) Have carry chains to have a better support for multi-bit operations iii) Have integrated memories, such as block RAMs in the devices we use iv) Have specialized units, such as Multipliers to implement functions that are Slow/ inefficient in CLBs [Configurable Logic Blocks] [6] FPGA enables high performance due to the following factors i)Tailoring to desired bit-width (ii) Ease of applying varying sample rates (iii) Flexibility of parallel execution of basic functions due to uniform architectural resources [7]

Here, two modules of Wi-Fi MAC layer transmitter are chosen and implemented on an FPGA device. The details of simulation are shown in tablet.

VI. SIMULATION RESULTS&DISCUSSION

The pay load data storage and data processing blocks consists of a total of five different individual modules i.e FIFO,Data length counter modules and serializer,HEC,CRC modules respectively all these modules are simulated using modelsim and simulation results are shown in fig 6.1a,6.1b,6.1c,6.1d and 6.1e

A. Simulation result of FIFO Module

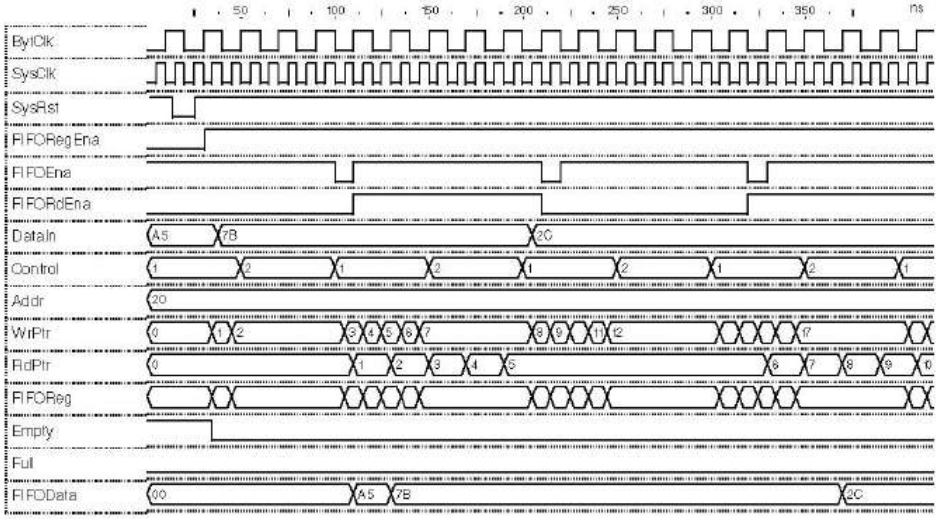

Fig 6.1a: Simulatio indicates enabling of FIFO on the raising edge of two clocks SysClk and ByteClk

B. Simulation results of Data length counter

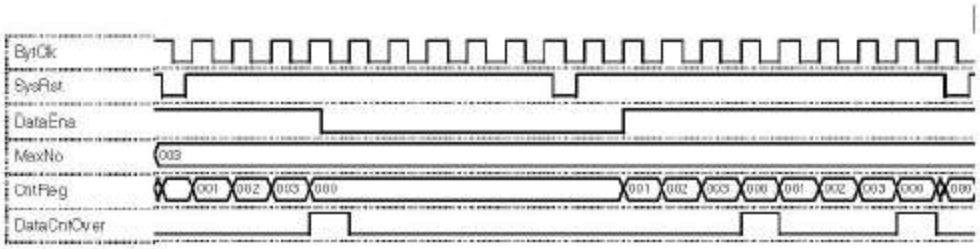

Fig. 6.1b: Simulation Indicate that, when the no of data is equal to the maximum number, then Data Cnt Over signal goes high

C. Simulation wave serializer module

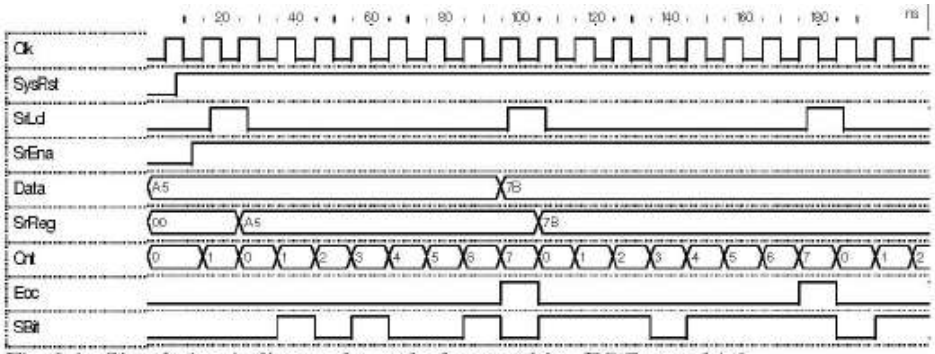

Fig 6.1c Simulation indicates the end of output bits, EOC goes high

D. Simulation results of HEC module

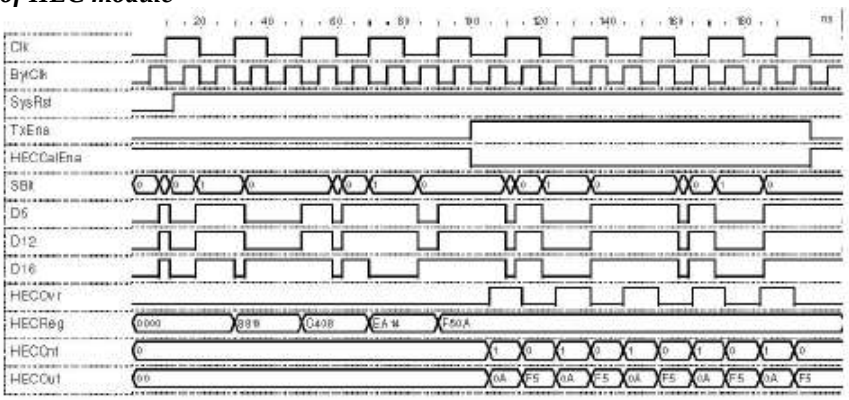

Fig6.1d: Simulation Indicates that when the T*Ena is high HEC Data is transmitted along with PLCP Header bits

E. Simulation results of CRC module

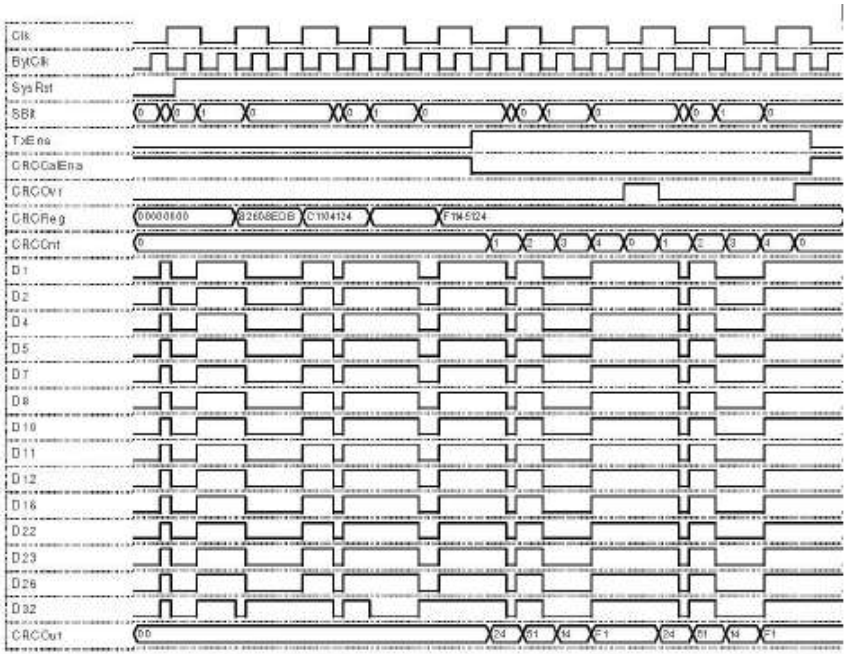

Fig 6.1e: Simulation indicate,at the end of transmission of data,CRC Over goes high

VII. CONCLUSIONS

Various individual modules of Wi-Fi Transmitter have been designed,verified functionally using VHDL-simulator,synthesized by the synthesis tool.This design of the Wi-Fi transmitter is capable of transmitting the frame formats. The formats include all 802.11 frames i.e. MAC frame, RTS frame , CTS frame and ACK frame. The transmitter is also capable of generating errorchecking codes like HEC and CRC. It can handle variable data transfer.

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