An Efficient Low Power Star Topology based NOC Router Architecture Design

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Abstract

Network-on-Chip (NoC) architectures represent a promising design paradigm to cope with increasing communication requirements in digital systems. Network-on-chip (NoC) has emerged as a vital factor that determines the performance and power consumption of many core systems. VLSI technology is to modify NOC internal router arrangements, shortest path allocation process and neighbor router estimation control. In existing paper the proposed design of 4*4 mesh topology based router architecture and to optimize the path allocation process using hybrid scheme which consist of VCS, CS, PS technique for path allocation work. This work is to reduce the data transferring time between source and destination. The existing system is consuming more power and to increase the circuit complexity level. Our proposed work is to design a 4*4 star topology based network on chip architecture. This work is to reduce the path allocation process using hop to hop data transfer technique. This technique is to increase NOC architecture performance level. This proposed architecture is to optimize the internal connectivity level and to reduce path allocation process level. This technique is to reduce data transfer time between source and destination. The proposed system is used to reduce the latency level and to improve throughput value.

Keywords: Low Power, Low Latency, STAR Topology NOC, Hop To Hop Data Transfer Technique

I. INTRODUCTION

Network On-Chip (NoC) has emerged as a scalable and promising solution to global communications within large multicore systems. In multicore system mainly based upon bitwise communication. Star networks are one of the most common computer network topologies. In its simplest form, a star network consists of one central switch, hub or computer, which acts as a conduit to transmit messages. This consists of a central node, to which all other nodes are connected; this central node provides a common connection point for all nodes through a hub. In star topology, every node (computer workstation or any other peripheral) is connected to a central node called a hub or switch. The switch is the server and the peripherals are the clients.

In Star topology, all the component of a network is connected through central device which is said to be hub. All the data on the star topology can pass through the hub before reaching the destination. Hub act as a junction to connect different nodes which is present in star network and at the mean time it manages and controls the overall network. Hub can also communicate with other hubs of different network.

Star topology based NOC router architecture gives better performance, signals don’t necessarily transmit to all networks. A sent signal reach the intended destination after passing through no more than 3-4 devices and 2-3 links. Performance of the network depends on the capacity of the central hub. It is easy to connect new nodes. In star topology networks new nodes can be added.
easily without affecting the rest of the network. Similarly, components can also be removed easily. Failure of the one node doesn’t affect the rest of the node. In the meantime, it is easy to detect the failure node and troubleshoot it. In star topology based NOC router architecture design which is used to optimize the latency as well as power.

The remaining part of this paper is organized as follows: in section II we describe the details about the previous work of our paper. Section III presents a brief description about star topology based NOC router architecture design with low power. Section IV presents simulation results of our proposed method. In section V presents our conclusions.

II. PREVIOUS WORKS

In [5] mesh topology NOC router architecture which is used to optimize the path allocation process using hybrid scheme. This hybrid scheme consists of Circuit Switched (CS), Packet Switched (PS) and Virtual Circuit Switched (VCS) technique for path allocation work. This work is used to reduce the data transfer time between source and destination. Implementing weighted distance based VCS technique and this technique is to optimize the internal path selection work. Using mesh topology based NOC router architecture it consumes more power and also increase the circuit complexity level as well as increase the latency level.

The hybrid scheme VCs which are exploited in Virtual circuit switching network in the form of number of VCS connections and multiple VCS connections which can be share by common physical channel. In this scheme CS and PS connections can transmit packets in which physical channel share more than one communication. Consider(x,y) denotes the physical channel from node to node. A physical channel can share by one CS connection and multiple PS connections. A VCS connection comprises VCs and routers that have been configured by recording in each router which input VC should be connected to which downstream VC. Crossbar switches of routers are preconfigured during the SA stage before VCS flits require passing through. Because VCS connections are established over VCs, a physical channel can be shared by VCS connections at most. Other communications competing for that physical channel must be executed in packet switching. In this mesh topology based NOC router architecture which increase the circuit complexity level and increase the latency level.

In the paper [3] we present a scalable many-core processor, intended for embedded applications. In XGRID, communication between cores is achieved via an FPGA-like interconnection network. FPGAs use rows and columns of buses with program. The specific XGRID processor, used in our experiments, is a 4x4 grid of 32-bit cores, each core having eight 32-bit ports. It has extracted a KPN and used the ILP approach, presented earlier, to obtain a mapping of the algorithm to our XGRID processor. It has used 2D DCT (Discrete Cosine Transform), MMUL (Matrix Multiplication), and four different versions of sorting benchmarks. Sorting algorithm benchmarks consist of the QSORT algorithm. Each core in XGRID has a limited number of ports, every communication channel in the KPN representation may not be mapped into XGRID. The KPN representation may need a modification to fulfill remaining requirements. The interconnect template creator decides whether or not to accept the ILP solution.

We explore the adaptation of conventional networking solutions to address two particular issues in next-generation Buffer less NoC design: congestion management and scalability. We Propose a new low-complexity and high performance congestion control mechanism in a buffer less NoC, motivated by ideas from both networking and computer architecture. To our knowledge, this is the first work that comprehensively examines congestion and scalability in buffer less NoCs and provides an effective solution based on the properties of such a design. The advantage is to consume less amount of power. The drawback is to increase the system complexity. Network performance may not accurately reflect system performance due to application-layer effects[4].

NOC require to increasing in delay and poor scalability issues in bus-based communication system architectures. A method using routing packets across multiple paths in NOCs based on path allocation algorithm can also reduce NOC congestion and bottlenecks which translates to reduce the frequency as well as power which increase the performance level[8].

NOCs using a dynamic programming network which improves in communication bandwidth and intelligent adaptation to faulty links and congested traffic. The dynamic programming network provide for optimal routing in NOC, this network provides shortest path computation using distributed dynamic programming. The result offers a new and effective solution for dynamic programming which enhance the performance of on-chip communication to reduce the power dissipation and also determines the area which is referred to be slices[9].

NOCs have been proposed as a very promising scalable communication paradigm SOCs. In this work presented a run-time reconfigurable framework based on the partial dynamic reconfigurable capabilities of Field Programmable Gate Arrays (FPGAs) which is used. Thus it is a promising framework to be applied to commercial NOC based SOC solutions which determines the latency NOC architecture[10].

III. PROPOSED METHOD

In our proposed work we can use star topology based NOC router architecture design. First we design a simple router internal architecture component. Router architecture is a memory storage function, this function is to store a source unit data bits. First we design a basic router internal elements and the router is consist of master-internal (source), slave routers memory, network interface, switch selection process, master-external (destination). These component are to construct the single router design work. Master and slave router memory is used to store the digital transmission data bits.
The master memory block is used to retrieve the destination data for the router architecture and to analysis the destination selection level also. The master process work is used to select the output data to the next node selection data. The single router architecture is to port the router architecture level and to check the master selection processing level. The single router design is to consists the three slave memory block in overall router architecture.

The slave position level is to check the another slave results and to analysis the previous data in another slave memory blocks. The slave memory block work is used to find next node data in overall NOC architecture. A common approach to relieve the problem consists of sharing most of network interface resources among a number of processor cores. The network interface architecture we are targeting supports multiple outstanding write transactions but only one pending read transaction. Our technique a promising solution for area efficient network-on-chip realizations across a range of operating conditions.

Circuit switched networks reserve a physical path before transmitting the data packets, while packet switched networks transmit the packets without reserving the entire path. The NOC architecture is a m × n mesh of switches and resources are placed on the slots formed by the switches. We propose a packet switched platform for single chip systems which scales well to an arbitrary number of processor.

Then to design the 4*4 router architecture and to apply the star topology connection between 4*4 NOC design. The 4*4 NOC design is to reduce the energy consumption level for inter and intra chip communication process. So we use the weighted bit calculation for every router placement position in 4*4 NOC design. The data transfer process is to analysis the all router position level and to find the shortest path between the source and destination router. So we check the low weighted bit level for nearest neighbor router estimation process. This process is to analysis the minimum router weighted bits. The neighbor router estimation control is used to check the shortest path identification control.

A. Block Diagram of Proposed System
The single router architecture is used to store the input data bits and to main the data bits using the clock signal. The router architecture is a one type of data storage and storage control process. The router section is used to maintain the signal energy level due to the long data transmission process.

The master memory block is used to retrieve the destination data for the router architecture and to analysis the destination selection level also. The master process work is used to select the output data to the next node selection data. The single router architecture is to port the router architecture level and to check the master selection processing level. The single router design is to consists the three slave memory block in overall router architecture. The slave position level is to check the another slave results and to analysis the previous data in another slave memory blocks. The slave memory block work is used to find next node data in overall NOC architecture.

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### B. Flow Diagram of Proposed System

![Flow Diagram of proposed system](image-url)
The flow diagram represents that giving source input 8-bit data to the router structure design process. The router structure design process consist of master internal and slave router design, network architecture process, switch design process and hop based master router external design. These component are to construct the single router design work. Master and slave router memory is used to store the digital transmission data bits.

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IV. RESULTS

The simulation result contain two stages: 1.data writing operation 2.data reading operation. In data writing operation we can give input 8-bit data to source router. In single router design process consist of master internal, slave 1,2,3 and master external. Then 4*4 router architecture design process using hop to hop router data transfer technique and this technique to reduce the path selection time. Hence, find the neighbor router estimation control and finally analysis the destination router design. Finally, simulate and synthesis the router architecture then those signals are transmitted. In data reading operation those signals are transmitted from source to destination using hop to hop data transfer technique.
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After synthesizing we can estimate the power using power estimator tool. The following figure give the power report we can vary the quick estimate and analyze it. Then the following table illustrates comparison table made on existing and proposed system design.
The main motivation of our work is to consume low latency and low power, then power will be 0.117w then the maximum frequency 876.194 MHz and time period is 1.141 ns.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>EXISTING SYSTEM</th>
<th>PROPOSED SYSTEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER (mW)</td>
<td>183.75</td>
<td>117</td>
</tr>
<tr>
<td>DELAY TIME (ns)</td>
<td>4.227</td>
<td>1.141</td>
</tr>
<tr>
<td>CLOCK FREQUENCY(MHz)</td>
<td>233.781</td>
<td>876.194</td>
</tr>
<tr>
<td>LATENCY (ns)</td>
<td>2</td>
<td>1.4</td>
</tr>
<tr>
<td>SLICES</td>
<td>805</td>
<td>441</td>
</tr>
</tbody>
</table>

The performance graph will be represented as a chart as following figure 7.

V. CONCLUSION AND FUTURE WORK

Thus the star topology based NOC router architecture provides a promising result which concentrates on reduction of power, delay and better performance is achieved. The power optimization in Xilinx tool gives a power consumption of 0.117mW and latency level of 1.4ns which is less compared to existing design. Future work is to design a torus network topology based 4 * 4 noc architecture using hop to hop router data transfer technique and this technique to reduce the path selection time. Torus network process is to effectively connecting all edge to edge router section. This section is to control the 3-layer of network architecture. router path allocation process is to applying the gray code algorithm.

REFERENCES