Single Stage and Two Stage OP-AMP Design in 180nm CMOS Technology

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Abstract

This paper presents the well define method for the design of single stage and two stage Op–amp in 180nm CMOS process. We have simulated diode connected load with two more PMOS to overcome trade-off between the output voltage swing, the voltage gain, and the input CM range. The operational amplifier has high gain, high input impedance and low output impedance. We have designed two stage op-amp of gain 72dB, CMRR 77dB, slew rate 133V/µs PSRR 57dB. Phase-margin 51˚.Design simulation has been carried out in NGSPICE.

Keywords: Operational Amplifier (OP-AMP), Complementary MOS (CMOS), Transistor logic (TTL). Metal oxide semiconductor (MOS), Common Mode Rejection Ratio(CMRR)

I. INTRODUCTION

The operational amplifier is one of the most useful and important component of analog electronics. They are widely used in popular electronics their primary limitation is that they are not especially fast the typical performance degrades rapidly for frequencies greater then about 1MHz, although some models are designed specifically to handle higher frequencies. We have designed an op-amp using CMOS technology. First we have designed one stage op-amp using CMOS technology and after simulation of it we have completed the process for two stage op-amp. We have simulated our circuit with NGSPICE simulation tool. We have design proposed topology using CMOS because it offer high gain and speed at low power consumption. MOSFETS have greater bandwidth. MOSFETS are considerably 'faster' than BJT's. CMOS ICs use much less power than TTL.

Section II describes the basic op-amp topology, section III describes the fundamentals of CMOS technology. The design and operation of single stage OP-AMP is discussed in section IV and the design and operation of two stage OP-AMP is discussed in section V. Finally, comparison and stimulation results of single and two stage OP-AMP illustrate in section VI.

II. BASIC OP-AMP TOPOLOGY

An op-amp is direct couple amplifier usually consisting one or more differential amplifier .The op-amp is versatile device that can be used to amplify DC as well as AC input signal and was originally design for performing mathematical operation such as addition, subtraction, multiplication and integration.[10]

The operational amplifier is an adjustable piece of equipment that can be used to amplify DC as well as AC input signals and was originally designed for performing mathematical operations such as addition, subtraction, multiplication, and integration. The input stage is a dual-input, balanced-output
differential amplifier. This stage usually provides most of the voltage gain of the amplifier and also establish the input resistance of the Op-Amp. [10]

In the middle of stage is usually another differential amplifier, which is driven by the output of the first stage. In most amplifiers the intermediate stage is dual Input, unbalanced (single-ended) output.

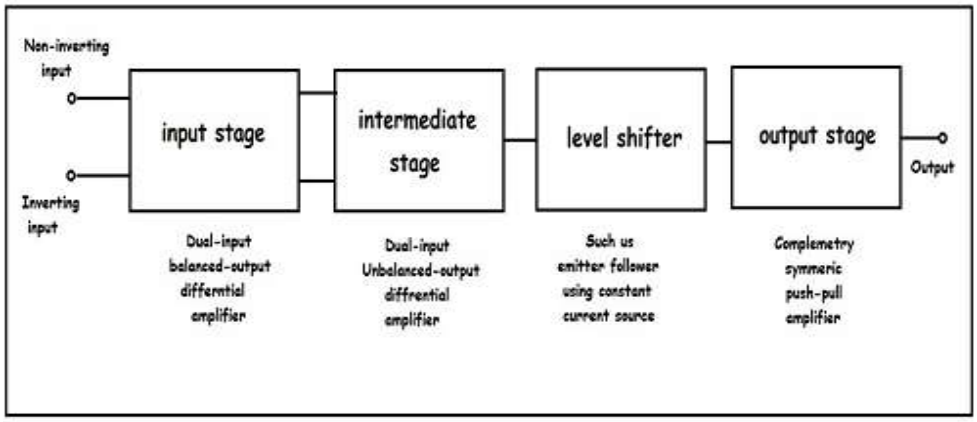


Fig. 1: Block diagram of a basic Op- amp

This is achieved by choosing a large size and high aspect ratio for the input pair. To reduce the flicker noise, we have changed a large (W/L) ratio.

The open loop gain of op amp determines the precision of the feedback system employing the op-amp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swing. [2]

III. FUNDAMENTALS OF CMOS TECHNOLOGY

A. CMOS (Complementary Metal Oxide Semiconductor):

CMOS semi-conductors use both negative polarity (NMOS) and positive polarity (PMOS) circuits. CMOS circuits more energy incapable since only one of these types of circuits can be on at a given time. This makes them particularly good-looking for use with handy electronics and devices that use battery power. [1]

B. N-Channel (NMOS) Transistors:-

NMOS transistors are negative polarity circuit components whose bulk consists of a p-well, typically created by the substrate. To make an n-channel transistor conduct, a positive voltage must be applied V_{GS} (gate reference the source) that is greater than the n-channel transistor's threshold voltage V_{TH}. The next issue is to make the current flow. It is possible for and yet has no current flow. To ensure the flow of current, a positive voltage must be applied V_{DS} (drain reference source). For this type of transistor the substrate must be connected to the most negative potential. [7]

For N-Channel transistors we use the following equations for the drain-source current, sat referring to the current when the transistor is in the saturation mode whereas without the sat subscript we are referring to the Triode mode. The same applies for the P-Channel.

$$I_{DSn} = (W / L)k'_n[(V_{GS} - V_{th}) - 0.5V_{DS}]V_{DS}$$

Where $k'_n = \mu_n C_{OX}$

$$I_{DSnsat} = (\beta_n / 2)(V_{GS} - V_{th})^2$$

Where $\beta_n = k'_n (W / L)$

C. P-Channel (PMOS) Transistors:

Since the source and drain of all CMOS transistors look alike, we must tell in what direction current is flowing to distinguish them. The source for a P-channel transistor is lower in the drain than in the source and vice versa for an N-channel. [7] Also for the NMOS, V_{GS}, V_{DS} and V_{TN} are typically positive whereas for the PMOS they are typically negative. The bulk of a PMOS is an n-well.

The equations for a P-Channel transistor are:

$$I_{DSp} = -(W / L)k'_n[(V_{GS} - V_{tn}) - 0.5V_{DS}]V_{DS}$$

$$I_{DSpsat} = -(\beta_p / 2)(V_{GS} - V_{tp})^2$$

IV. DESIGN AND DESCRIPTION OF SINGLE STAGE OP-AMP

A single-ended signal is defined as one that is measured with respect to a fixed potential usually the ground. A differential signal is defined as one that is measured between two node that have equal and opposite signal excursions around a fixed potential the two types of signal contently.

An important advantage of differential operation over signal-ended signaling is higher protection to environmental noise. The sensitive signal is distributed as two equal and opposite phase. The noise involvement of M_1-M_4, as calculated in all op-amp topologies at the input noise in the two input transistor and two load transistor. [2] Design of single – ended diode connected current source is as shown in figure 2.

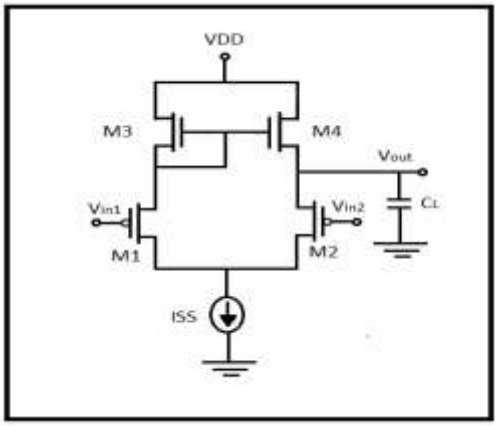


Fig. 2: Signal-ended diode connected current source

Now consider the transient load current, I_L, due to a modify in V_{IN}. Write the differential equation that relates V_{OUT} and I_L, and then delay it to solve for VOUT as a function of I_L. To increase the voltage gain we have modified the circuit as shown in figure3.

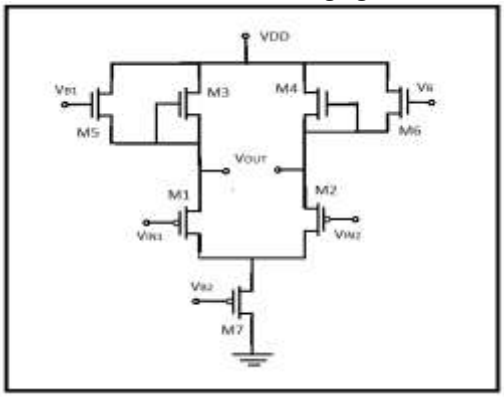


Fig. 3 Modified circuit to increase the voltage gain

The copying operation and reference generator circuit Thus if this voltage is applied to the gate and source terminal of second MOSFET. The resulting current is I_{OUT}= I_{REF}. Form another point of view; two identical MOS devices that have equal gate-source voltage and operate in saturation carry equal current.

The structure of M1and M2 is called ”current mirror”. In the general case, the devices need not be the same. Neglecting channel –length modulation .MOSFET can be use as current when it is operated in saturation as shown in figure4.

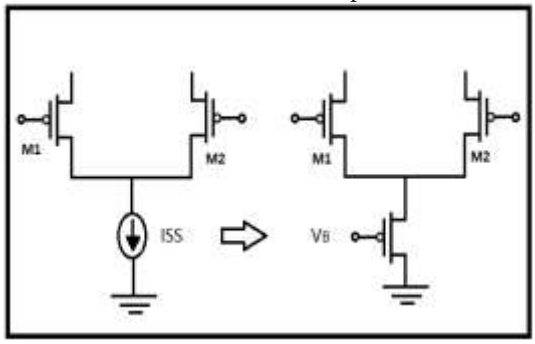


Fig. 4: Current mirror circuit

V. DESIGN AND DESCRIPTION OF TWO STAGE OP-AMP

In some applications the gain and/or the output swing provided by cascade op amps are not sufficient. In such cases, we alternative to "two-stage" op amps, with the first stage provided that a high gain and the second, large swing. In contrast to cascade op amps, a two-stage configuration isolates the gain and swing requirements.

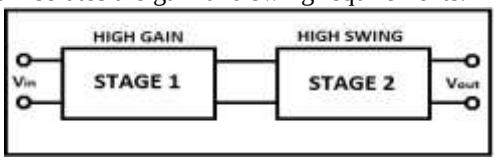


Fig. 5: Two Stages

As shown in fig 5, 1st stage will provides high gain and 2nd stage will provide high swing. We have simulated two stage op-amp topology as show in fig.6

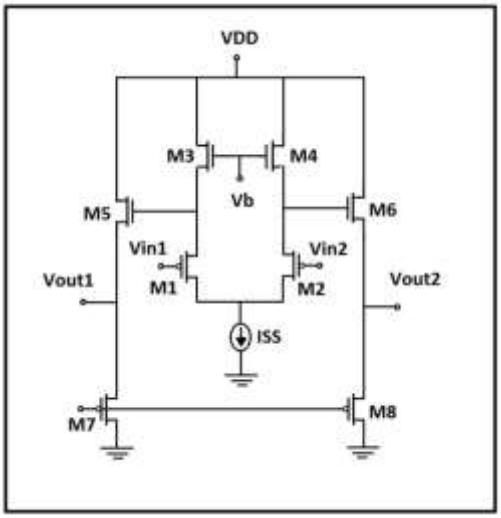


Fig. 6: Two stage op-amp

VI. COMPARISON AND SIMULATION RESULT

Comparison of single stage and two stage are illustrated in Table 1.

Table – 1
Comparison Table

Design Specification	*Single Stage OP-AMP*	*Two Stage OP-AMP*
Technology	*180nm*	*180nm*
Supply voltage	*3.3V*	*3.3V*
Dc gain	*36dB*	*72dB*
Output swing	*4.5V*	*5.6V*
CMRR	*39dB*	*77dB*
Slew rate	*75V/µs*	*133V/µs*
PSRR	*30dB*	*57dB*
Power dissipation	*1.3mV*	*1.8mV*
Capacitance	*1pF*	*1pF*
Phase margin	*68°*	*51°*

A. AC Analysis:

Using AC analysis we achieved the gain, phase margin and CMRR.
Gain =72dB, CMRR=77dB, PSRR=57dB

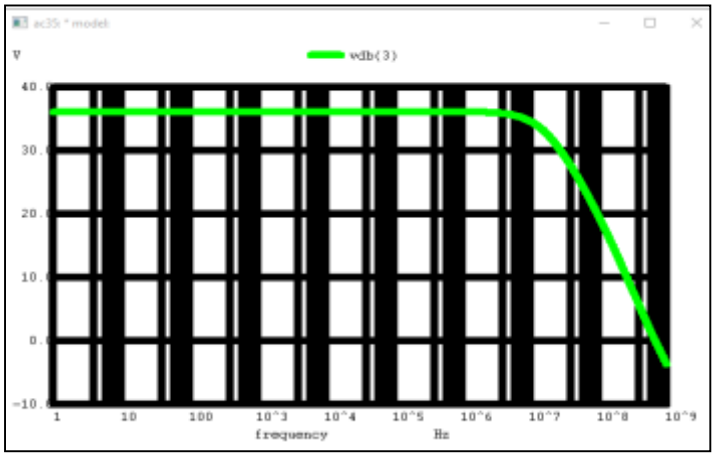


Fig. 7(a)

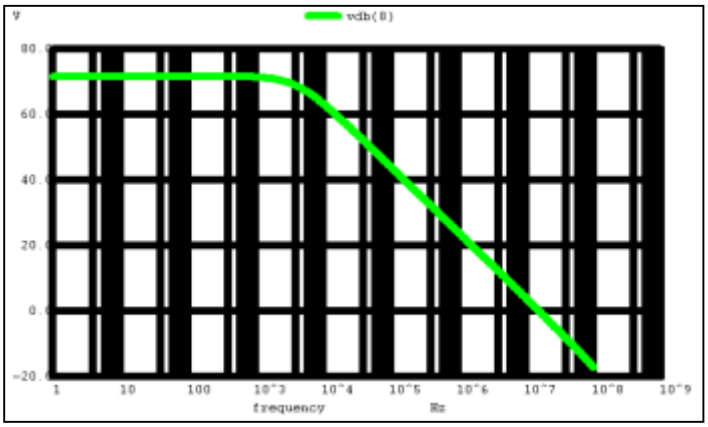


Fig. 7(b):

Fig. 7: (a) AC analysis of single stage OP-AMP (b) AC analysis of two stage OP-AMP

Slew rate of single stage and two stage is calculated using the transient analysis as shown in figure 8(a) and 8(b) respectively.

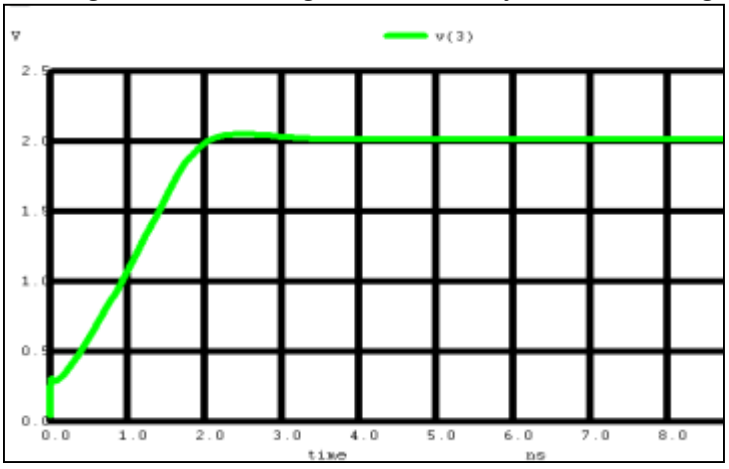


Fig. 8(a):

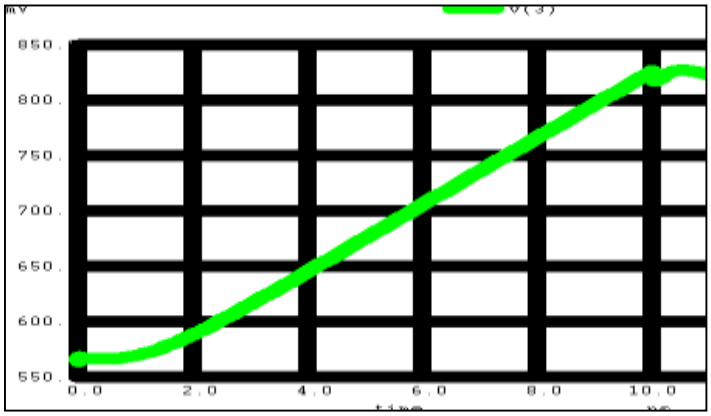


Fig. 8 (b)

Fig. 8: (a) slew rate measurement of single stage OP-AMP (b) slew rate measurement of two stage OP-AMP

Phase margin of single stage and two stage is calculated using the transient analysis as shown in figure 9(a) and figure 9(b) respectively.

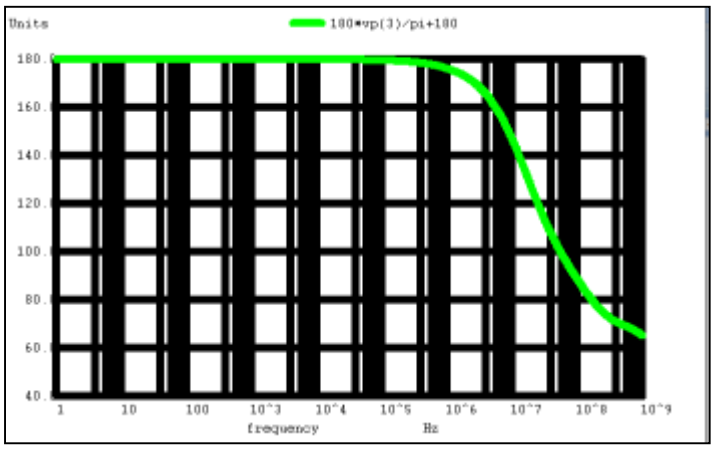


Fig. 9 (a)

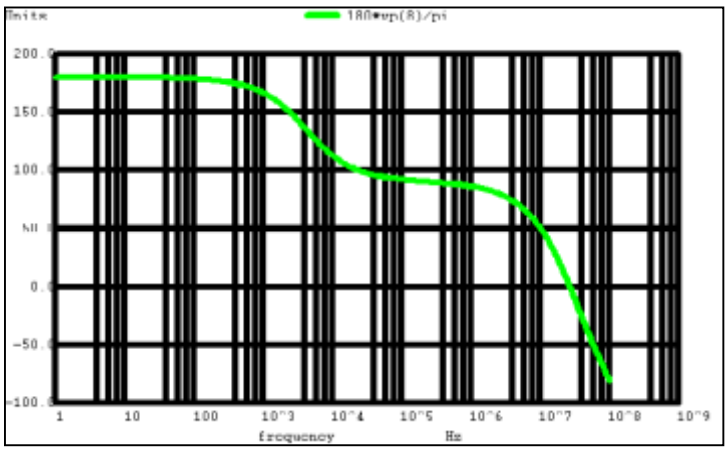
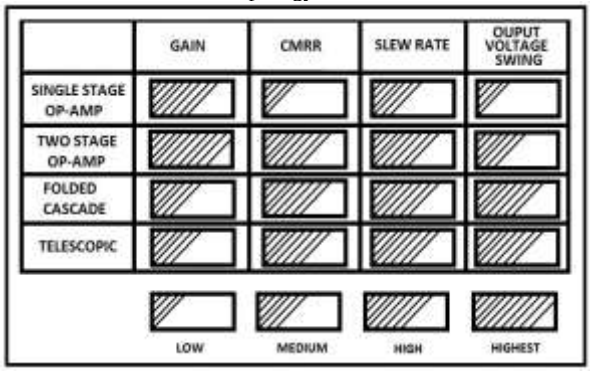


Fig. 9 (b):

Fig. 9: (a) Phase margin measurement of single stage OP-AMP (b) Phase margin measurement of two stage OP-AMP

Comparison of various op-amp topologies reported in [2] is as given in table-2.

Table – 2
Various topology of OP-AMP



VII. CONCLUSION

Various architectures were explored for the implementation of OP-AMP. We have design and stimulate single stage and two stage OP-AMP in 180nm CMOS technology using NGSpice stimulation tools the simulation of two stage OP-AMP shows CMRR(77dB), GAIN(72dB),SLEWRATE(133V/us),PSRR(57dB),Power dissipation(1.8mV), Output swing(5.6V) and phase margin (51°).

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