Design of Low Power Carry Select Adder by using VHDL

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Abstract

In digital circuitry, fast adder is required to carry out computations in various chips like DSP processors. Carry Select Adder (CSLA) is one of the fast adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, there is scope for reducing the area and power consumption. This uses a simple and efficient gate -level modification to significantly reduce the area and power of the CSLA. Based on this modification 32-bit CSLA architecture has been designed and compared with the 32-bit conventional CSLA architecture. The modification uses Binary-To-Excess-1Converter logic instead of the chain of Ripple carry adder where the carry bit is 1.This logic has less number of gates as compared to the design without using binary to excess 1 converter logic. The modified circuit is designed and verified on Xilinx ISE design suite 14.3.The power is calculated on Xilinx Power Estimator tool. The area comparison is completed with respect to respect of LUTs .Proposed design has reduced area and power as compared with the conventional CSLA. The thesis evaluates the performance of the design in terms of area and power. The result analysis shows that the proposed CSLA structure is quantitatively superior over standard CSLA in terms of area and power.

Keywords: CSLA, RCA, BEC, VHDL, XILINX ISE

I. INTRODUCTION

In recent digital circuits, an adder is needed that consumes less area and power with comparable speed. Adders in circuits acquire large space and consume massive power as massive additions are done in advanced processors and systems. Adder is one amongst the key hardware blocks in Arithmetic and logic unit (ALU) and digital signal processing (DSP) systems. Principally the digital process needs high speed and low power multiplier accumulator (MAC) unit. Addition and multiplication are the most vital operations in this unit. The DSP applications where an adder plays a vital role include convolution, digital filtering like in discrete Fourier transform (DFT) and fast Fourier transform (FFT), digital communications and spectral analysis. Specifically, speed and power efficient implementation of these adders could be a terribly difficult problem.

A. Carry Select Adder (CSLA):

Carry Select Adder is considered to be the good design choose for high speed and having reasonable area. The main difference between Carry Select Adder and Ripple Carry Adder is that in a Ripple Carry Adder the carry has to ripple through full adders and every full adder cell has to wait for the incoming carry before an outgoing carry can be generated, but in the case of carry select adder the carry has to pass through the single multiplexer. The principle of carry select adder is that ,at each level we have two adder units .Each unit implements the addition operation in parallel as shown in figure(1).

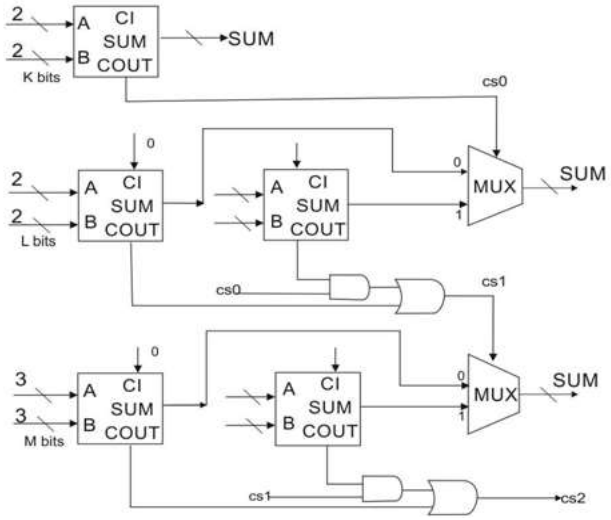

Fig. 1: Carry Select Adder using multiplexer

B. Ripple Carry Adder(RCA):

The CSLA is used in many computational systems to alleviate the problem of carry propagation the delay by independently generating multiple carries and then select a carry to generate the sum. But, the CSLA is not area efficient because it uses multiple pairs of ripple carry adders(RCA) to generate partial sum and carry by keeping in mind carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexer(MUX).

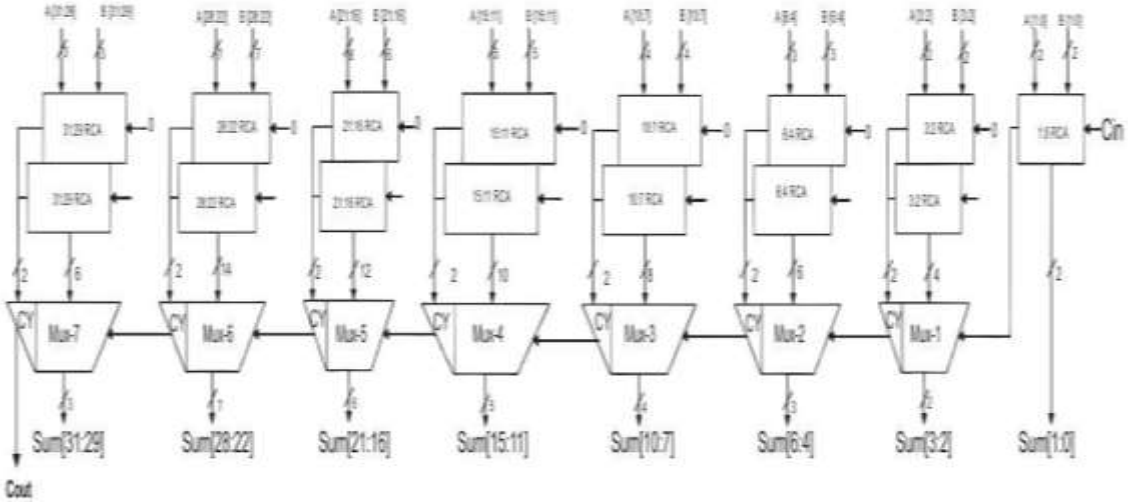

Fig. 2: Regular 32-bit Carry Select Adder

II. BINARY TO EXCESS-1 CONVERTER (BEC)

The basic idea of this work is to use binary to excess-1 converter(BEC) instead of RCA with Cin=1 in the regular CSLA to obtain lower area and power consumption .The main advantage of this BEC logic comes from the lesser number of logic gates then the n-bit full adder(FA) design. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-bit BEC are shown in figure no-4 and table no-2 respectively.

Figure no-3 illustrates how the basic function of the CSLA is obtained by using 4-bit BEC together with the MUX. One input of the 8:4 MUX gets as in input (B3, B2, B1&B0) and another input of the MUX is the BEC output. This produces the two possible partial results in parallel and the MUX is used to select either the BEC output or the direct input according to the control signal Cin. The importance of BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The design expressions of the 4-bit BEC are listed as:

X0=~B0
X1=B0^B1
X2=B2^ (B0&B1)
X3=B3^ (B0&B1&B2).
(NOTE: The functional symbols ~ NOT, & AND,^XOR)

Table – 1
Function Table of the 4-b BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

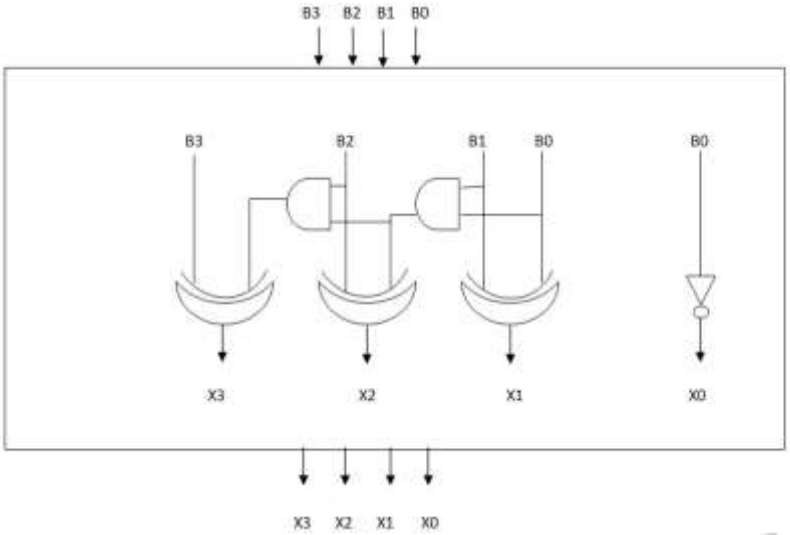

Fig. 3: 4-Bit BEC

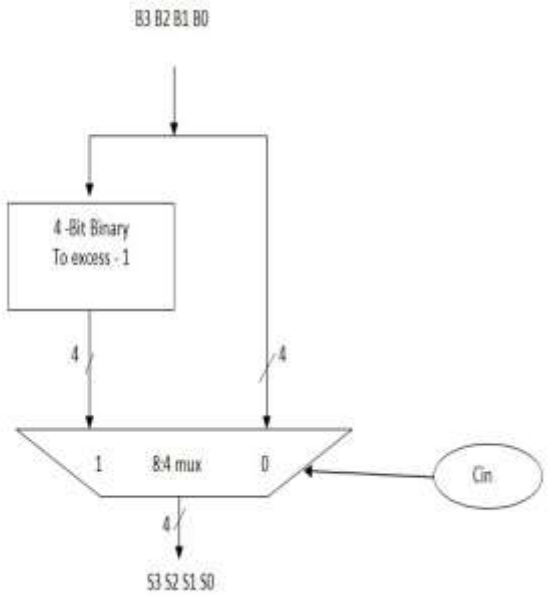

Fig. 4: 4-Bit BEC with 8:4 MUX

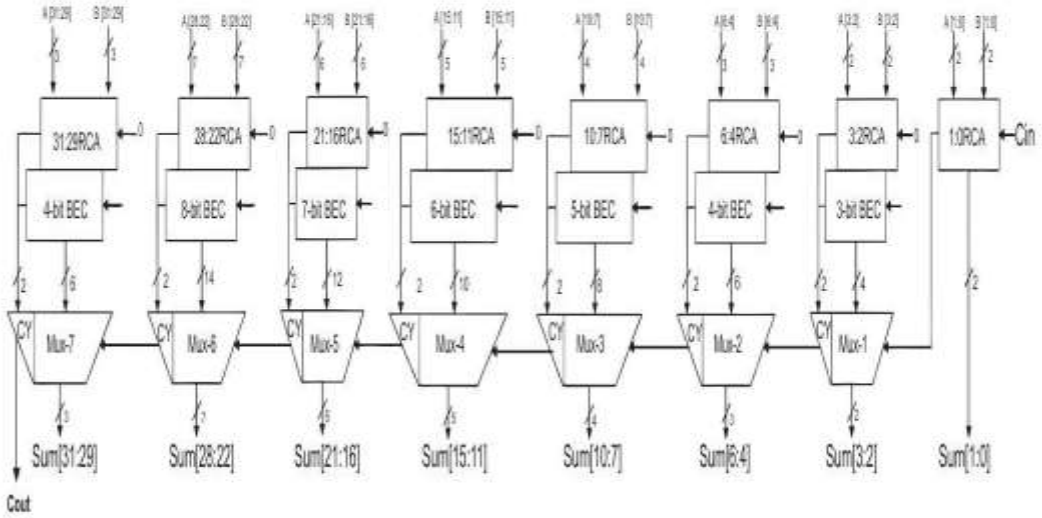

Fig. 5: Modified 32-Bit CSLA. Parallel RCA with Cin=1 is replaced with BEC

III. SIMULATIONS

Fig. 6: Simulation result of Regular 32-bit Carry Select Adder

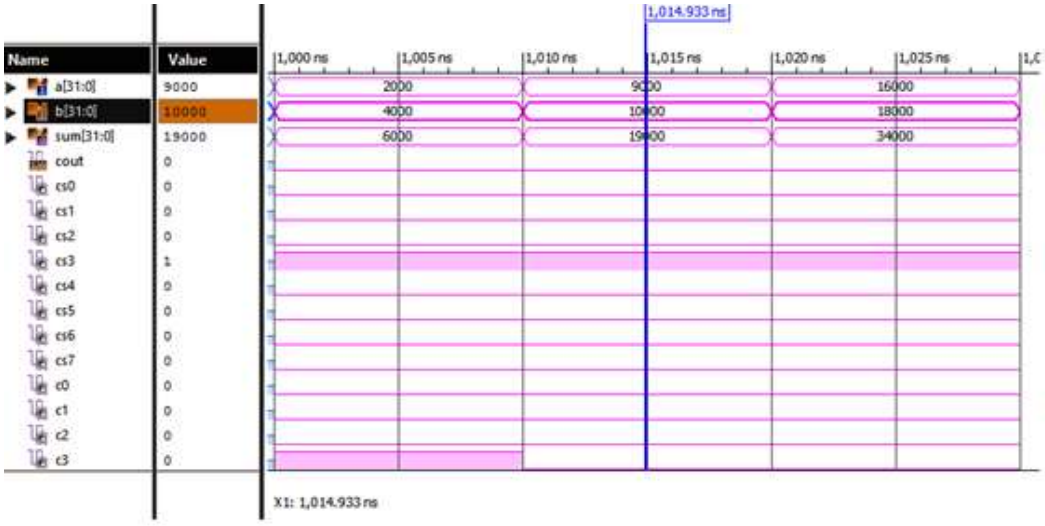

Fig. 7: Simulation result of Modified 32 bit Carry Select Adder

IV. RESULTS

Table – 2
Comparison of the Regular and Modified CSLA results tested for Spartan6XC6SLX16

ADDER	*AREA*	*DELAY*	*TOTAL POWER(W)*
Regular 32-bit CSLA	*No. of 4 input LUT'S-101 out of 9312*	*23.118nsec*	*0.178W*
Modified 32-bit CSLA	*No. of 4 input LUT's-97 out of 9312*	*21.809nsec*	*0.143W*

- The Power Modified 32 bit Carry Select Adder is reduced by 19.66%.
- The Delay of Modified 32bit Carry Select Adder is reduced by 5.66%.
- The Area of Modified 32bit Carry Select Adder is reduced by 3.96%.

V. CONCLUSION

- A simple approach is proposed in this work to reduce the area and power of carry select adder architecture.
- The reduced no of the gates of this work offers the great advantage in the reduction of the area and also the total power.
- The compared result shows that the modified carry select adder has reduced power approximately upto 20 %.
- The area factor of the proposed design shows a decrease for 32 bit sizes which indicate the success of this work.
- The modified carry select adder architecture is therefore low power and low area, simple and efficient for VLIS hardware implementation

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