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High Performance Mac Design using Vedic Multiplier and Reversible Logic Gate

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Abstract

Multipliers are effective in many applications; the performance of system is directly proportional to throughput of the multiplier. The system depended throughput of multiplier and a system became slow therefore we need to design high performance multiplier. In this paper we implement The Vedic Multiplier and the Reversible Logic Gates and Accumulate Unit (MAC) Urdhava Triyagbhayam sutra for design of Vedic multiplier and the adder design is done by using reversible logic gate. Reversible logics are also the fundamental requirement for the emerging field of Quantum computing. The analyses result shows that our multiplier is faster than conventional multiplier and compares delay required for multiplier operation and also compare power and area of multiplier.

Keywords: Reversible Logic, Urdhava Triyagbhayam, Quantum Computing, Kogge Stone Adder, Gates

I. INTRODUCTION

Recently, Multipliers are effective in many applications like as microprocessor, digital signal processing and most often used in critical arithmetic unit in many applications such are Fourier transform, discrete cosine transforms and digital filtering operations. The throughput of these applications mainly depends on multipliers. When the multiplier operations are too slow in the circuit, then the performance of the entire circuits will be reduced. In the accumulate adder the previous MAC output and the present output will have added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. The main advantages of Multiply-Accumulate (MAC) unit are logic units, digital signal processors and microprocessors, since it finds the speed of the overall system [13]. The efficient designs by MAC unit are Nonlinear Computation like FFT/IFFT, Discrete Cosine or wavelet Transform (DCT). Therefore, it is basically use for multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Basically the delay, mainly critical delay, created due to the long multiplication process and the propagation delay is found because of parallel adders in the addition step. The main aim of this paper is comparison of area, speed and other parameters of Conventional MAC unit with the Vedic MAC design.

II. PAPER CONTRIBUTION

A multiplying function is in three methods: partial product Generation (PPG), final conventional addition and , partial product addition (PPA). The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit, where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra. Multiplication is the fundamental operation of MAC unit [1]. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two major criterion that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path. The second part of MAC is Reversible logic gate. In modern VLSI, fast switching of signals leads to more power dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy are generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc.

III. DESIGN OF MAC ARCHITECTURE

For design of MAC architecture, we required 3 sub design

1) Design of 32×32-bit Vedic multiplier.
2) Design of adder using DKG gate reversible logic.

3) Design of accumulator which integrates both multiplier and adder stages.

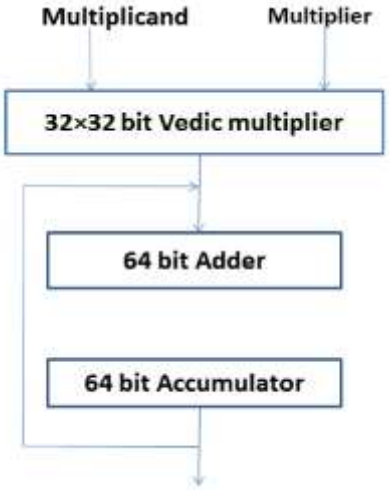

Fig. 1: Modified MAC Architecture

IV. VEDIC MULTIPLIER

The Vedic mathematics applicable over complex calculation, it reduces the typical calculation into a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

A. Urdhva Tiryakbhyam Sutra

The Vedic multiplier is depends on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "*Vertically and Crosswise*". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

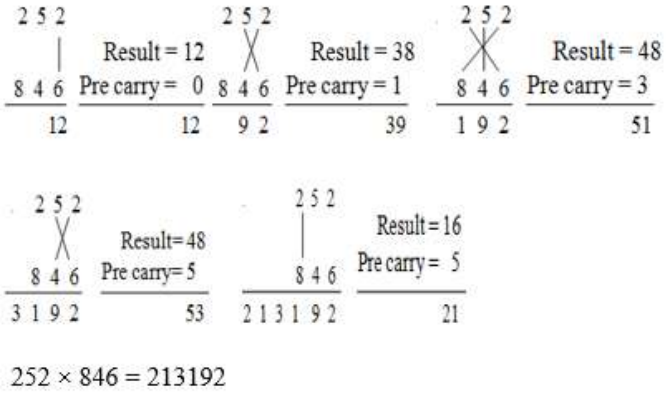

Fig. 2: Multiplication of two decimal numbers –252 x 846

B. Vedic Multiplier for 2x2 Bit Module

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by

multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

s0 = a0b0;
c1s1 = a1b0 + a0b1;
c2s2 = c1 + a1b1;

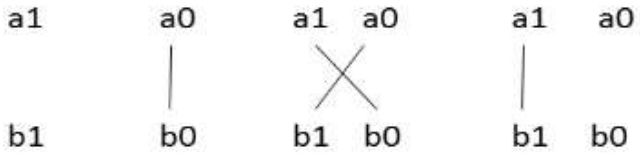

Fig. 3: The Vedic Multiplication Method for two 2-bit Binary Numbers

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [2].

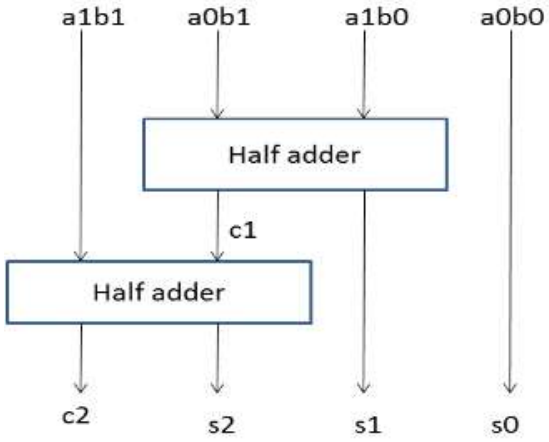

Fig. 4: Block Diagram of 2x2 bit Vedic Multiplier

C. *Vedic Multiplier for 4x4 bit Module*

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3. Let's analyze 4x4 multiplications, say A= A_3 A_2 A_1 A_0 and B= B_3 B_2 B_1 B_0. The output line for the multiplication result is – S_7 $S_6S_5S_4$ S_3 S_2 S_1 S_0. Let's divide A and B into two parts, say A_3 A_2 & A_1 A_0 for A and B_3 B_2 & B_1B_0 for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2-bit multiplier block, we can have the following structure for multiplication as shown in Fig. 4.

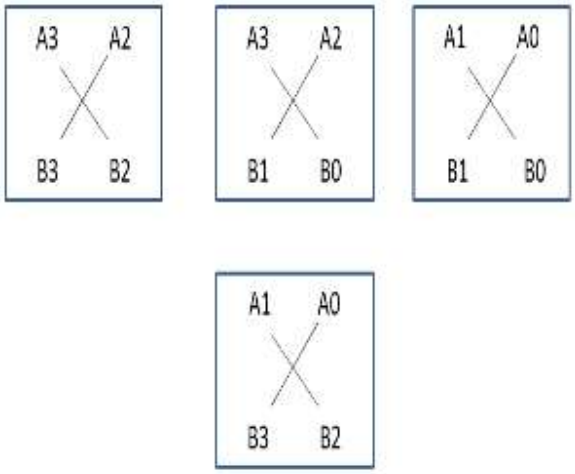

Fig. 6: Sample Presentation for 4x4 bit Vedic Multiplication

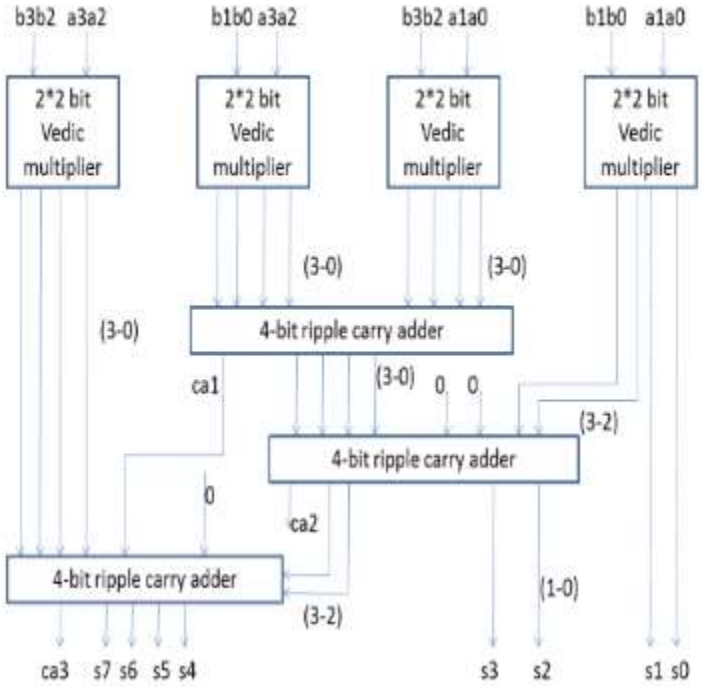

Fig. 7: Block Diagram of 4x4 bit Vedic Multiplier

D. 32 x 32 bit Vedic Multiplier

Using a 16×16 Vedic multiplier we can design 32 ×32 Vedic multiplier with carry save adder as shown in fig.3. We have modified the final adder stage with the Kogge stone adder which is more efficient than the Carry save adder which is shown in the fig

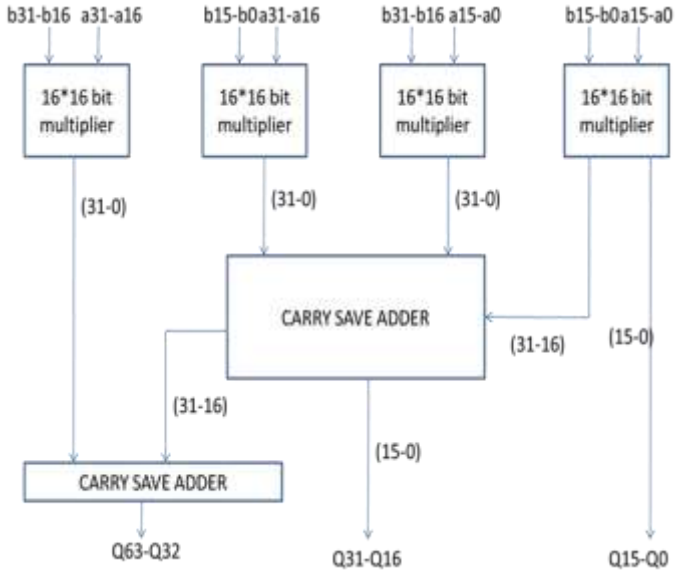

Fig. 8: 32 × 32 Vedic Multiplier with Carry save Adder

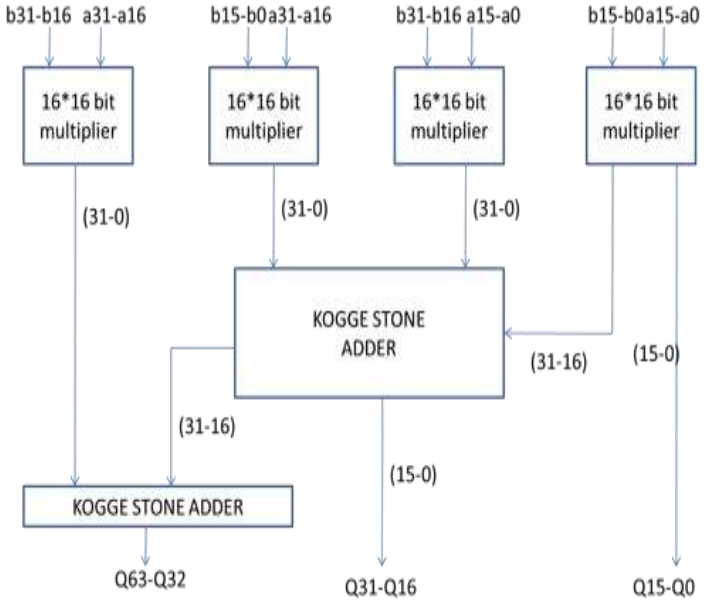

Fig. 9: 32 × 32 Vedic Multiplier with Kogge Stone Adder

V. REVERSIBLE LOGIC

Reversible logic is a unique technique (different from other logic). Loss of information is not possible in here. In this, the numbers of outputs are equal to the number of inputs.

A. General Consideration for Reversible Logic Gate

A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer [18] proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet [17] showed that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

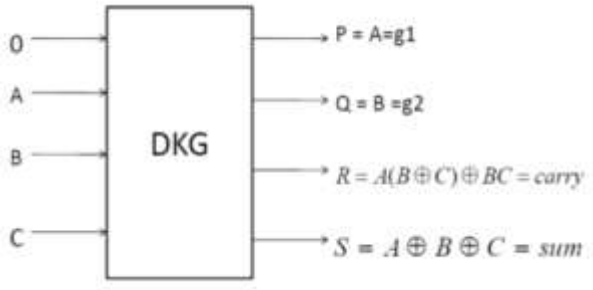

Fig. 9: DKG gate as a Full adder

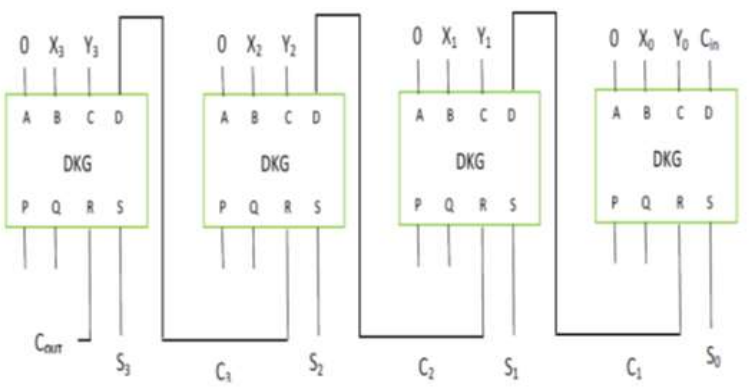

Fig. 10: Parallel adder using DKG gate

VI. ACCUMULATOR STAGE

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance when compared to the pervious MAC designs.

VII. RESULTS

The modified multiplier using the Kogge Stone Adder is fast and the design of 32-bit MAC is done in Modelsim. The synthesis is performed out in Cadence RTL compiler. The bove design is implemented in Verilog Code using mentor graphics modelsim 6.5b. Comparison of area, speed and power reports is made with other methods as shown in table.

parameter	*Booth multipler*	*Booth recorded vallace tree multiplier*	*Vedic multiplier with KOGGE stone adder and reversible adder*	*Vedic multiplier and reversible adder*
Power (nw)	*18846.5*	*17936.4*	*15686.4*	*15567.7*
Speed(ns)	*7.12*	*6.92*	*5.21*	*5.68*
Area(um2)	*2408*	*2376*	*2054*	*2157*

The RTL view and simulation result of MAC is shown in fig. 11 and fig. 12 below.

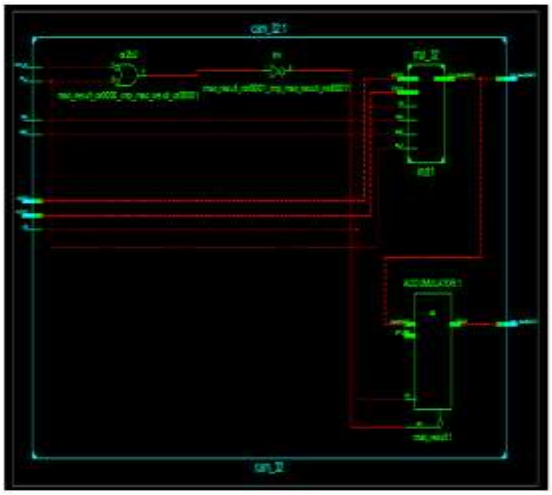

Fig. 11: RTL schematic of 32-bit MAC architecture

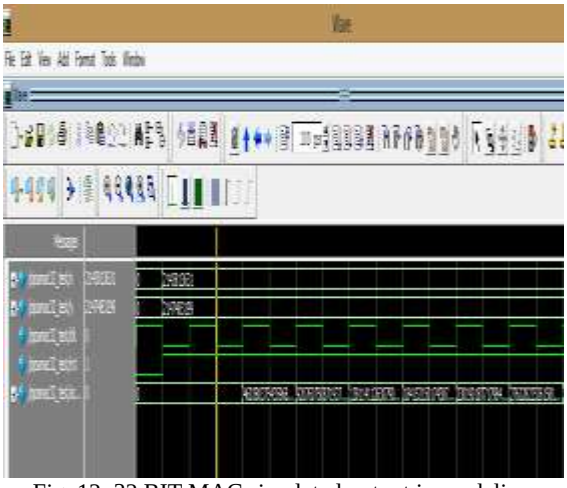

Fig. 12: 32 BIT MAC simulated output in modalism

VIII. CONCLUSION

In this paper we implement high performance multiplier with reversible logic and compare speed, power and area, from this result it indicate that this architecture has useful over conventional multiplier and it increases the performance of circuit. The Urdhava Triyagbhayam and reversible logic is very useful over conventional multiplier in all expect like power, speed and area.

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