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Efficient Adders

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Abstract

Half adders are used to add two one bit numbers. In order to add two one bit numbers with the carry generated in previous order addition, we use full adders. For adding multiple bit wide numbers, we cascade full adders to form Ripple Carry Adders (RCA). RCA is one of the area efficient adder, but it is not much faster because of the carry propagation delay. Carry Select Adders (CSLA) use two RCA blocks, one generates partial sum by assuming carry-in as zero and the other assumes carry-in as one. The original sum output is selected by using multiplexers after the carry-in from previous order additions obtained. The modified CSLA replaces the RCA block with carry-in one by a Binary to Excess One Converter(BEC). This paper proposes an efficient adder which is a modified CSLA without multiplexer, were we replace the multiplexer and BEC with a combination circuit consisting of XOR and AND gates.

Keywords: BEC, CSLA, RCA

I. INTRODUCTION

In electronics, adder is used to perform addition of numbers[3]. In processors adders are used in ALU, because all the arithmetic operation can be done using adders. Subtraction can be represented by one's complemented addition, multiplication by multiple additions, and division by multiple subtractions. The adders are not only used in ALU, but also used to calculate addresses, table indices[2][3] etc. Adders are used in high speed integrated circuits and in digital signal processing[1][2] for executing FFT, FIR and IIR Algorithms[3][6].

As we know the adders are used in many computer systems and mobiles, where millions of instructions are executed per second, speed is an important constraint while designing a system. When considering the portability of the device it must be smaller in size and should not consumes much power. The design of systems with less area, power and delay is are of considerable importance in the area of research[4][5]. In adders, carry propagation delay reduces the speed of addition[2][4][5].

For single bit additions we use full adders. For multiple bit wide additions, we concatenate full adders to form RCA.RCA is much area efficient but it is not much efficient in terms of the speed. This is because of the carry has to propagate from one stage to other. So each full adder has to wait until carry from previous addition arrives.

In CSLA we reduce the delay by using dual RCA blocks [1], where one RCA assumes carry-in as zero and the other assumes carry-in as one[2][4][5]. In both RCA blocks, partial sums and carry are generated and given to the corresponding multiplexers, where the correct sum and carry are selected when the original carry arrives. In Conventional CSLA, difference between RCA blocks is only that one computes sum assumes carry-in as zero and other assumes Carry-in as one. We can get the output of RCA block with carry-in one by adding one with the output of RCA block with carry-in zero. This can be done by using Binary to excess one converters. BEC converts the Binary input value to its excess one value. This is the concept of modified CSLA[2].

In modified CSLA without mux, we replace the RCA block with carry-in one and the multiplexers by simple combinational circuits[5] consisting of AND and XOR gates.

II. ADDERS

A. Ripple Carry Adders

The full adder adds three one bit numbers which is often represented as A, B and Cin. A and B are the operands and Cin is the carry generated from the previous stage. The adder produces two bit output, sum(S) and carry(C_{out}) which is represented as:For an n bit adder,n full adder circuit should be cascaded ie,the carry generated in previous order addition is given to the Cin input of next full adder.So each carry bit is rippled through stages,thus it is called ripple carry adder. In ripple carry adder, the carry-out bits of each full adder stage should be carried out as the carry-in of the next full adder stage. In Ripple Carry Adder the carry signal has to be rippled from the least significant stage to the most significant stage to get the Most Significant Bit (MSB). So the final sum and the carry bit will be valid only after some delay.

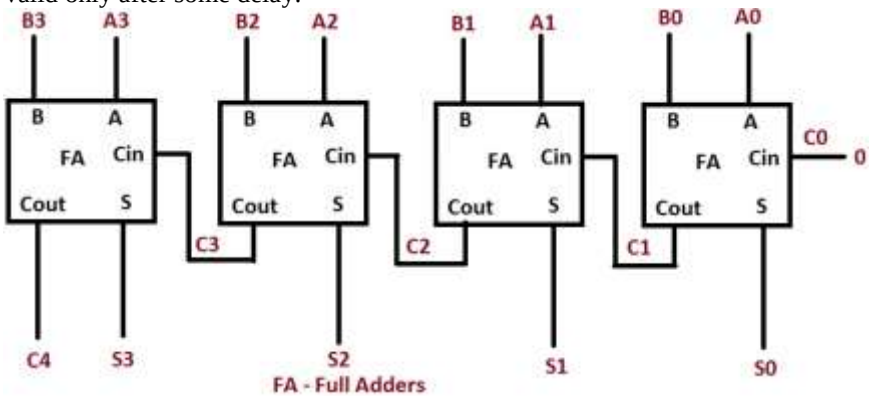

Fig. 1: Ripple Carry Adder

Fig 1. shows the basic block diagram of a Ripple Carry Adder with Full adders.Ripple carry adder is the one of the area efficient adders but it has more delay because of the carry propagation.For a n bit ripple carry adder,output can be obtained after n Full adder delays.

B. Conventional CSLA

Conventional CSLA is a combination of two Ripple Carry Adders and a Carry and Sum Selection Unit.It uses dual RCA blocks.

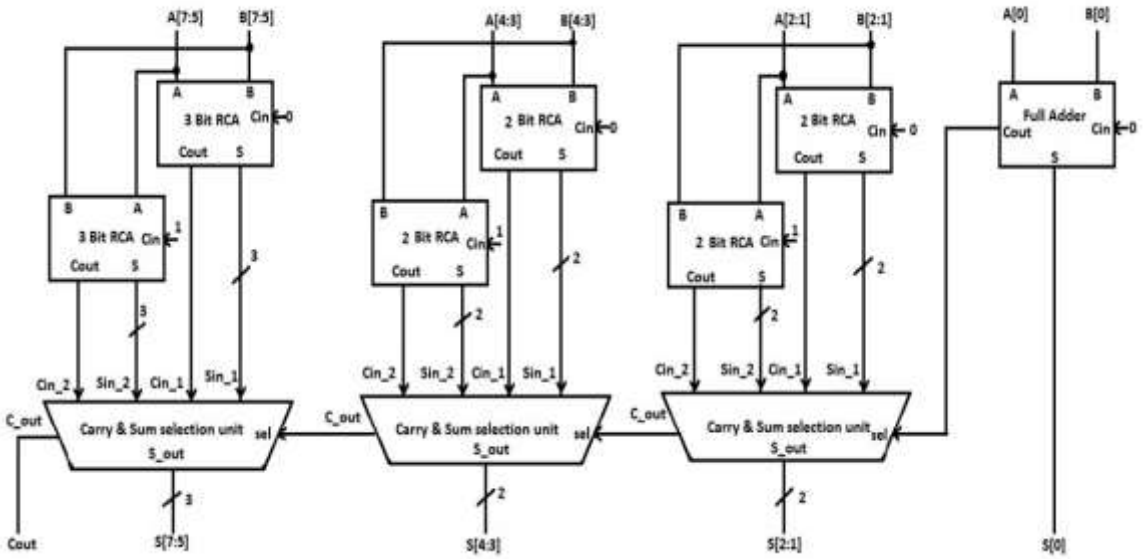

Fig. 2: Conventional CSLA

In ripple carry adder each full adder waits until the carry out from the previous order addition arrives. Carry select adder uses two block of ripple carry adders, one of which adds the two bits with fixed zero carry-in and other add two bits with carry-in one. Every RCA blocks will run in parallel. The partial sum and carry generated by RCA block is selected after actual carry-in arrives. This is done by a carry and sum selection unit. Carry and sum selection unit is a combination of two multiplexers, one of which is used to select sum and other is used to select carry. The both multiplexers have same select line, i.e. the carry out of previous order addition.

Fig 2. shows the internal structure of Conventional CSLA which consist of two ripple carry adders and a Carry and Sum Selection Unit. The truth table of a carry and sum selection unit is shown in Table 1.

Table - 1
Truth Table of Carry and Sum Selection Unit

INPUT					*OUTPUT*	
Sin_1	*Sin_2*	*Cin_1*	*Cin_2*	*Sel*	*S*	*Cout*
0	*0*	*0*	*0*	*0*	*0*	*0*
0	*0*	*0*	*0*	*1*	*0*	*0*
0	*1*	*0*	*1*	*0*	*0*	*0*
0	*1*	*0*	*1*	*1*	*1*	*1*
1	*0*	*1*	*0*	*0*	*1*	*1*
1	*0*	*1*	*0*	*1*	*0*	*0*
1	*1*	*1*	*1*	*0*	*1*	*1*
1	*1*	*1*	*1*	*1*	*1*	*1*

The sum and carry-out equations for a conventional CSLA is as follows:

S=(Sin_1&(~Sel))+(Sin_2&sel) and Cout=(Cin1&(~Sel))+(Cin2&sel)

C. *Modified CSLA*

In CSLA, the output of RCA block with carry-in one can be obtained by adding one with the output of a RCA block with carry-in zero. So by finding a circuit which is more efficient and having the same output RCA with carry-in one, we can improve the performance of the adder. The BEC can the used instead of RCA with carry-in one. BEC converts the input value to its excess one value. To replace the n-bit RCA, n+1 bit BEC is required. So by using a modified CSLA which consists of one RCA block and BEC and Carry and Sum Select Unit, area can be reduced than a conventional CSLA. One input to the carry and sum select unit is sum along with carry output from RCA and another input to the carry and sum select unit is the sum along with carry output from BEC circuit. The final sum and carry outputs are selected depending on the select line of the carry and sum select unit, which is the carry-out from previous order addition.

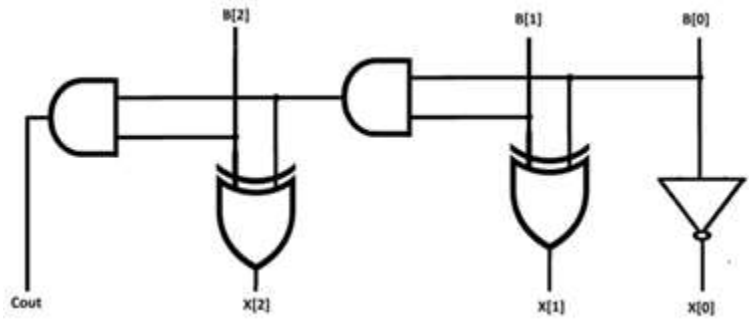

Fig. 3: Binary to Excess 1 Converter

Table - 2
Truth Table of BEC

Binary logic B0 B1 B2	*Excess 1 logic X0 X1 X2*	*Carry*
000	*001*	*0*
001	*010*	*0*
. . . .	. . . .	. . . .
110	*111*	*0*
111	*000*	*1*

Fig 3. shows the internal diagram of a three bit Binary to Excess One Convertor followed by its truth table in Table 2. Fig 4. shows the internal diagram of Modified CSLA which consists of a Ripple Carry Adder, Binary to Excess One Convertor and a Carry and Sum Selection Unit.

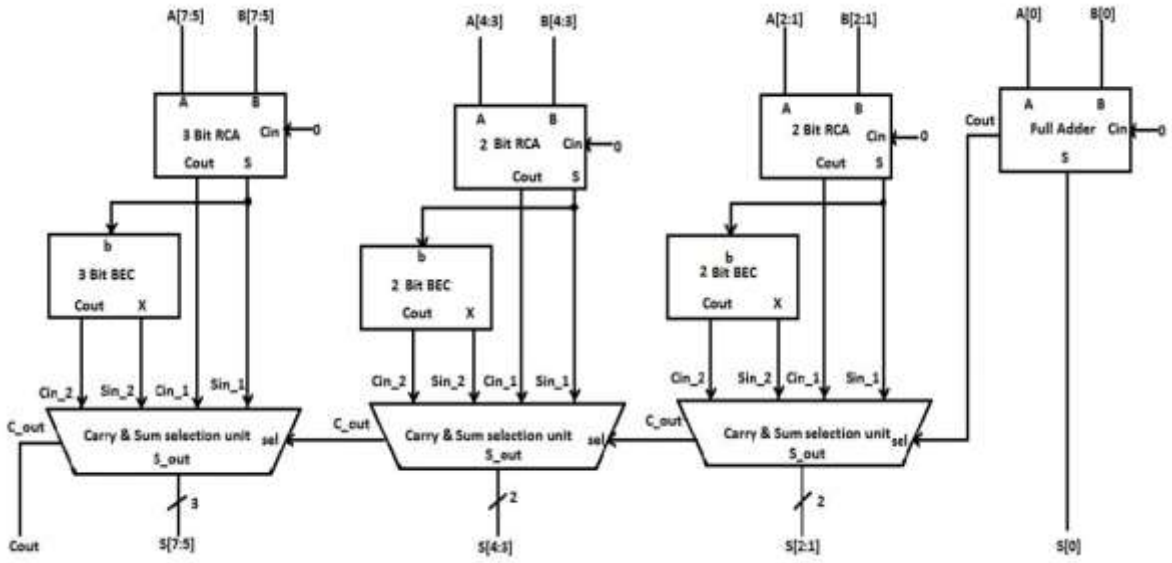

Fig. 4: Modified CSLA

D. Efficient Adder

Efficient Adder is a modified CSLA without MUX, were replace a RCA block with carry-in one and the multiplexers by simple combinational circuit containing XOR and AND gate. The combinational circuit is capable of adding and selecting correct sum according to carry-out from previous order addition.

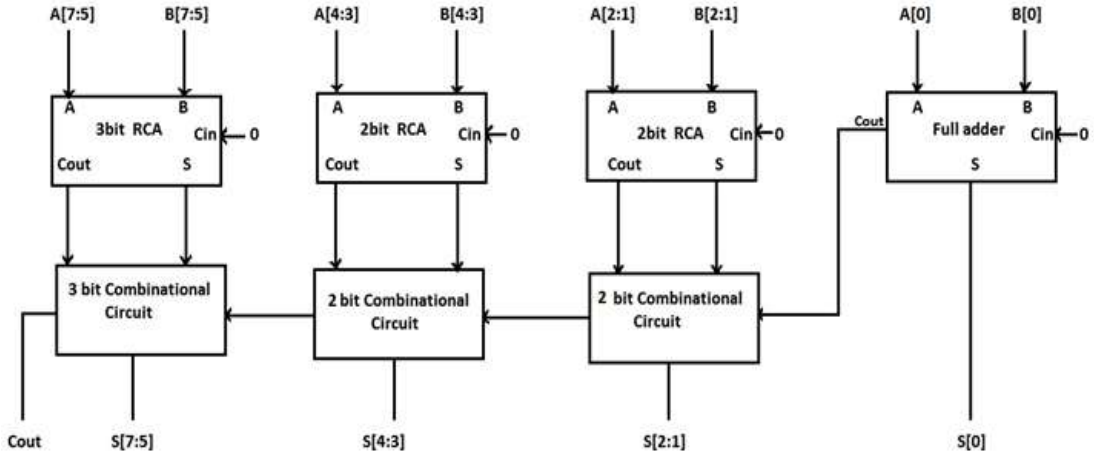

Fig. 5: Modified CSLA without mux

Fig 5. Shows the internal diagram of an Efficient Adder which consists of full adder, Ripple Carry Adder, 2-bit combinational circuit and a 3-bit combinational circuit.

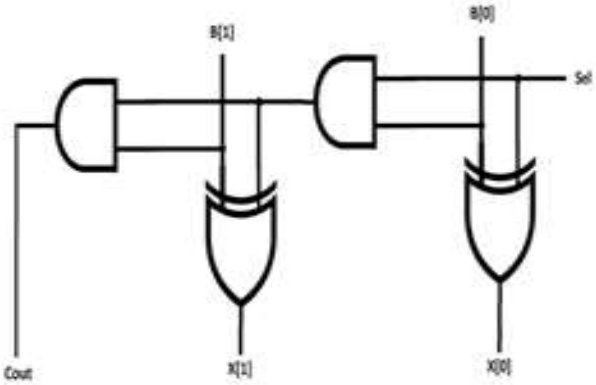

Fig. 6: 2 Bit Combinational Circuit

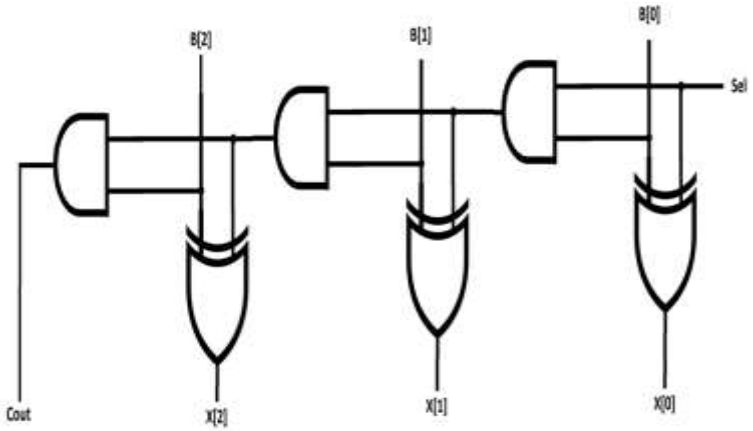

Fig. 7: 3 Bit Combinational Circuit

The Combination circuit produces excess one value of the input applied to it if the Sel signal is one. If the Sel signal is zero, the combinational circuit produces output same as that of the input applied to it. By using this technique, we can reduce the area and power of the CSLA with little excess delay than conventional CSLA. But its delay is less than that of the ripple carry adder. Fig 6. and Fig 7. shows the internal diagram of a 2-bit and 3-bit combinational circuit respectively.
The equations for a combinational circuit are as follows:
X[0]=B[0]⊕ sel X[1]=B[1] ⊕ (B[0].sel) X[2]=B[2] ⊕ (B[1].B[0].sel) Cout=B[2].B[1].B[0].sel

III. RESULT

This work has been developed using Xilinx ISE 8.1i tool. Table 3 shows the comparison between Delay, Power and Power Delay Product of various adders such as 8- bit Ripple Carry Adder,8-bit Conventional CSLA,8-bit Modified CSLA,8-bit Efficient Adder.

Table - 3
Comparison of Adders for Delay, Power and Power Delay Product

Adder	*Delay(ns)*	*Power(mW)*	*Power Delay Product*
RCA	*16.191*	*6.60*	*106.8606*
Conventional CSLA	*15.85*	*12.60*	*199.71*
Modified CSLA	*13.269*	*9.29*	*123.26*
Efficient Adder	*16.080*	*6.60*	*106.128*

IV. CONCLUSION

In VLSI design process, power, delay and area are the important factors that determine the performance of any circuit. The Ripple Carry Adder is the one of the area efficient adder, but it is not much speed efficient. RCA has a problem of carry propagation delay. The Carry propagation delay in RCA can be overcome by using Carry Select Adder. But conventional CSLA has the disadvantage of more power consumption and large area. In Modified CSLA we overcome this problem by replacing RCA block with carry-in one by using BEC block. In Efficient Adder we can reduce area and power and make it simple to implement.

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