Design of Index based Round Robin Arbiter for NOC Router

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Abstract

Network-on-chip (NOC) is one of the scalable on-chip communication systems which are used to meet the communication demands of large number of System on chip (SoC) cores. In NOC architecture, router is a main factor which transmits data from source to destination. In router design, arbiter is important due to its performance and efficiency of NOC systems. Round robin arbiter (RoR) is a type of arbiter used in router; there are 3 different existing designs of round robin arbiter such as Parallel round robin arbiter (PRRA), Improved PRRA (IPRRA) and High speed and decentralized round robin arbiter (HDRA) and there is a high demand for low power consumption, low delay and high speed operations. Hence, in this project we proposed an Index based round robin arbiter (IRRA), which works with an index format of the input ports to reduce the power consumption, delay of the circuit. The proposed method is compared with PRRA and HDRA for delay and power consumption. Finally, the minimum number of optimizing parameters such as delay and power consumption is achieved. The design of Index based round robin arbiter is coded in Verilog, synthesized and simulated in Xilinx ISE Design Suite 12.4 tool.

Keywords: Round robin arbiter, IRRA, Delay, Power consumption

I. INTRODUCTION

In today's VLSI trend, area and speed are big challenges on single chip, where many number of processing elements (PEs) are placed on System on chip (SOC). There are different types of interconnection schemes that are currently in use like crossbar, buses and NOCs. NOC is used to improve the scalability and power reduction in a complex circuit. In Network on chip, router is the main factor which routes the input data from source to destination. During routing if many inputs requests for the same destination then arbiter is the one which selects the inputs according to their provided priorities. Round robin arbiter is a type of arbiter which works under the principle of recent served should have least priority in the next cycle or next round of arbitration.

Using round robin arbiter algorithm there are different types of arbiters which are implemented already, some of those are Parallel round robin arbiter (PRRA), Improved parallel round robin arbiter (IPRRA) and (HDRA) High speed and decentralized round robin arbiter. We are proposed an Index based round robin arbiter (IRRA) which has inputs in the form of index format to reduce the delay and power consumption. According to the arrangement of indexed inputs the outputs are executed. Here we are considering two previously designed round robin arbiters such as Parallel round robin arbiter (PRRA) and High speed and decentralized round robin arbiter (HDRA) to compare with proposed Index based round robin arbiter (IRRA) for delay and power consumption.

II. BASIC CONCEPT OF NETWORK ON CHIP

A. Network-on-chip (NOC)

Network-on-chip (NOC) is a new communication concept that solve the problem that challenges the SOC. NOC provides technologies for generic on-chip interconnection by routers which connects processing elements (PEs) like ASICs, FPGAs, memories and IP cores, network interfaces (NIs), and routers. The data of PEs which are used for communication are packetized using NI and transferred through on-chip network each PE is attached to NI which connects PE to local router. When packet is sent from source PE to destination PE, the packets are forwarded by network via the route which is decided by each router, NOC architecture is shown in below figure 1.

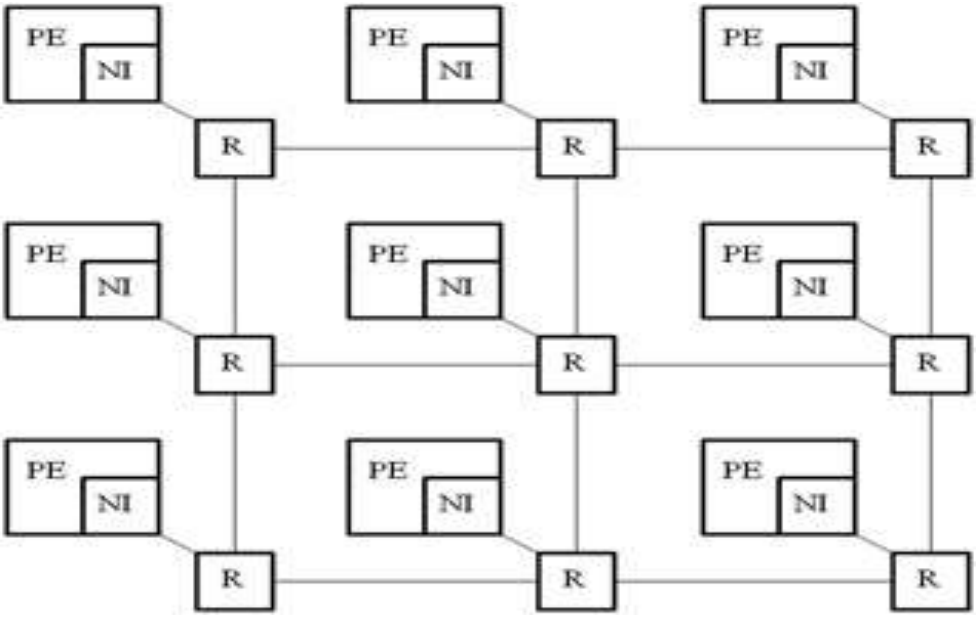


Fig. 1: Typical NOC architecture

B. Router

The heart of on-chip network is the router, which is responsible for performing the crucial task of coordinating the data flow from requested source to destination. NOC router consists of three main blocks they are crossbar, buffer and arbiter which is shown in below figure 2.

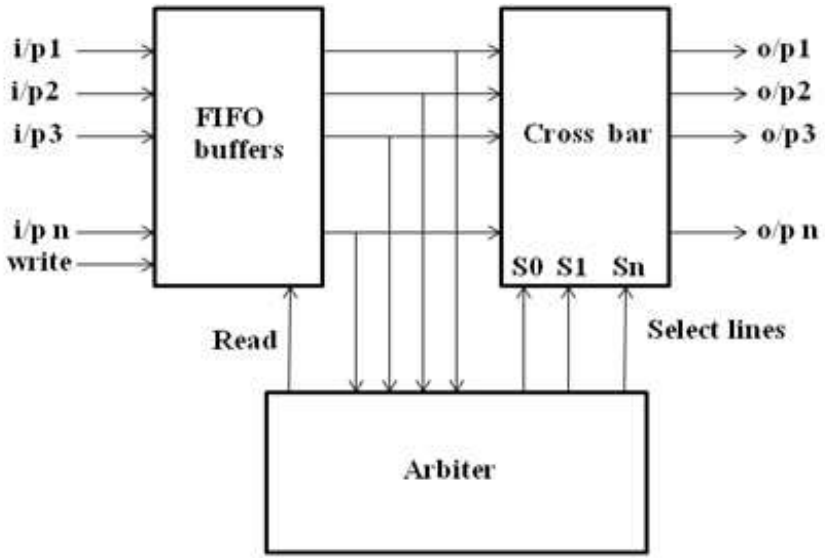


Fig. 2: Block diagram of NOC router

NOC switches need to provide high speed and cost effective, when many number of packets from different input port requests for the same output port then a fast arbiter is one of the most important factors for high performance NOC. The primary factor which limits the power consumption is by physical interconnection on a chip. Rapid increase in switching speed of crossbar switch leads to problem, which is resolved by implementing a fast and fairness arbiter to maximize the switch throughput and performance for NOC.

III. METHODOLOGY

A. Parallel round robin arbiter

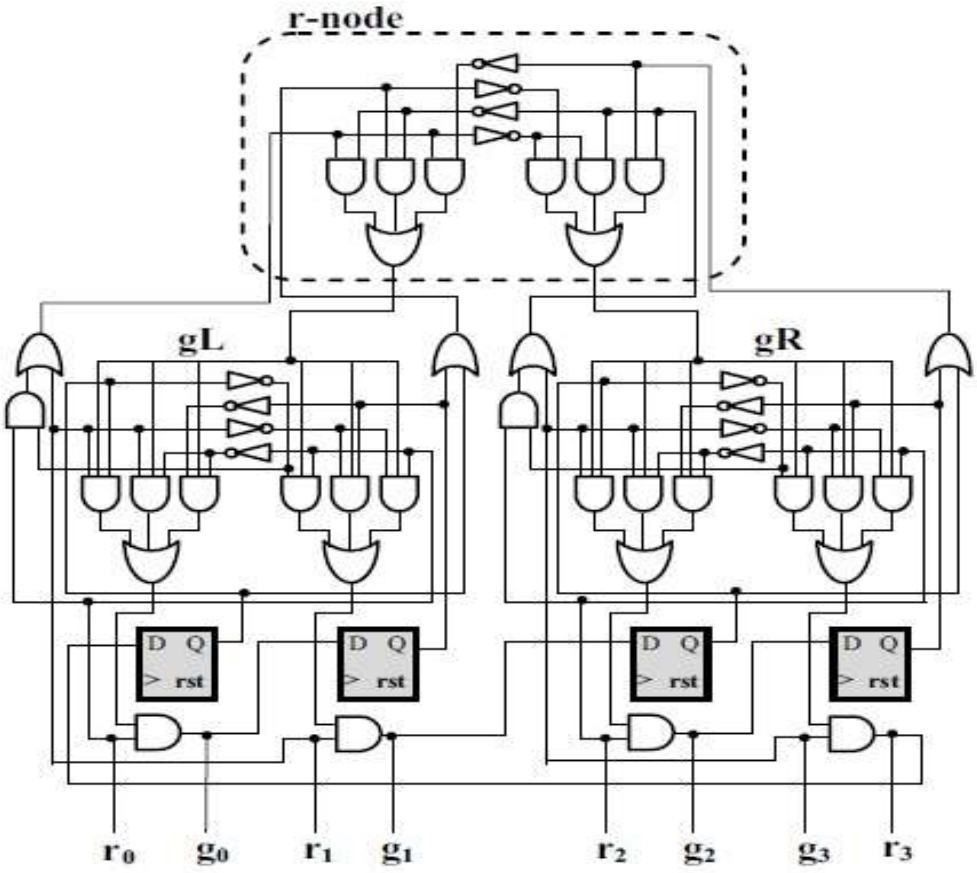


Fig. 3: 4- input PRRA architecture

Above figure 3 represents the Parallel round robin arbiter (PRRA) which is based on simple binary search algorithm. Implementation of binary search algorithm helps in hardware implementation and it is easy to implement in hardware. PRRA is a combinational circuit with an implementation of binary tree structure. PRRA arbitration is divided into up-trace and down-trace. Up-trace is one of the subprocess of collecting the input requests along with their priorities information of round robin. Down-trace is another sub process which is used for the decision making with the information collected about input request and priorities in up-trace. Up-trace is further divided into grant left (gL) and grant right (gR).

B. High speed and decentralized round robin arbiter

High speed decentralized round robin arbiter (HDRA) is designed in such a way that it reduces the power consumption, delay and circuit area compared to other designs. Figure 4 is the HDRA architecture, all the inputs are applied to the individual dash circles where dash circle acts as a filter circuit hence it is also known as filter circuit. This dash circle will filter the currently executed request and it gives chance to the next request. Filtering of request by dash circle is done only when act signal is high. Act signal is the important factor in HDRA architecture, with act signal as low no output is executed.

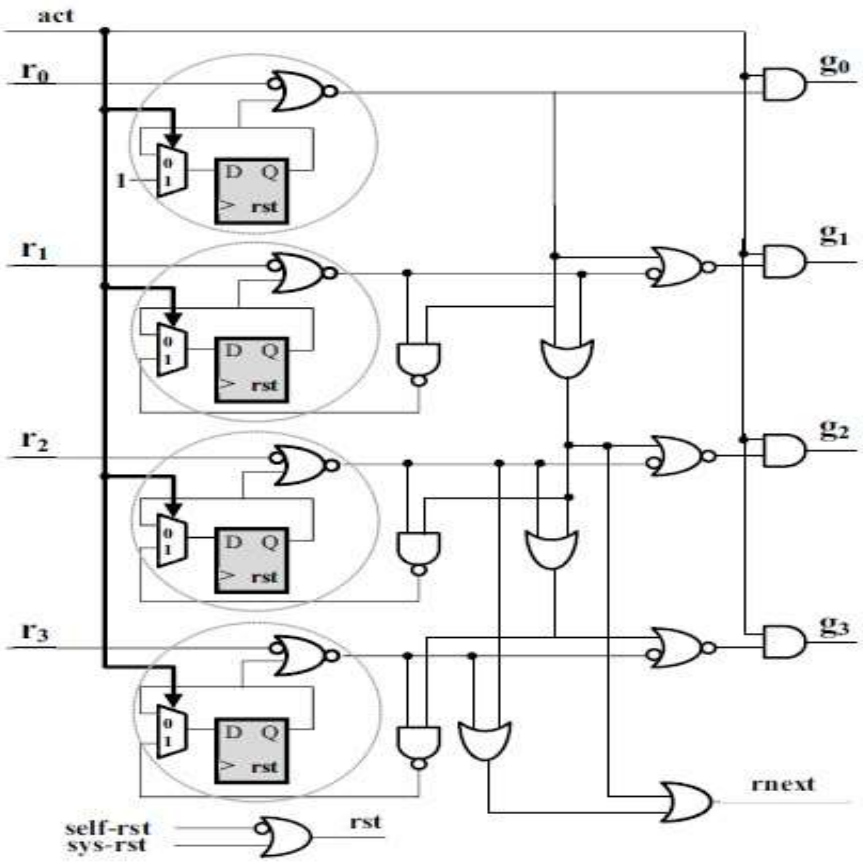


Fig. 4: 4-input HDRA architecture

C. *Existing index based round robin arbiter*

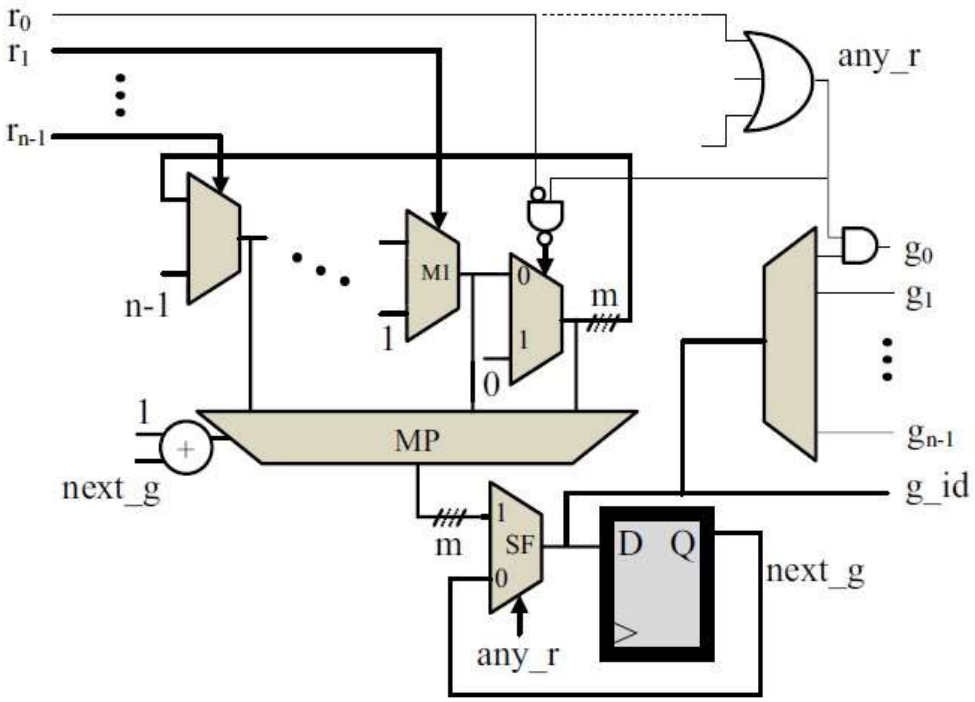


Fig. 5: Circuit of existing IRRA

Above figure is the circuit diagram of the Index based round robin arbiter all inputs are applied to the individual mux along with the index which is applied to the mux. All the outputs from the respective mux are applied to the signal mux named MP. The

output of the mux MP is given as input to the SF mux which has another input as 0 and select line is the ORing of all inputs. D flip flop stores the data and gives the output as next_g. the output of D flip flop is fed back to MP mux to identify currently executed input and it is also incremented by 1 to indicate that to give execution chance for the next input.

The output of SF mux is considered as the output of the design but it is in a single output which is called as grant index (g_id). This gives only single output but not n outputs as that of inputs hence g_id is applied as input to the demux which intern decode the output into n outputs. If there is no input request then all the inputs are operated with OR gate and ANDed with grant signals to avoid the errors from the previous output. Hence to avoid the additional ANDing of signal with grant signal, new IRRA is proposed which reduces the delay, power consumption and area than an existing IRRA.

IV. PROPOSED METHOD

Figure 6 is the block diagram of proposed index based round robin arbiter and figure 7 is the circuit diagram of proposed IRRA. Each input are in the index format which is applied to each individual multiplexer. Number of outputs from all individual multiplexers is sorted out to a single output by a mux MP. In a proposed IRRA, instead of demux for decoding of output decoder is used. Decoder gives the error free output when there is no input request whereas demux was sending with some error of the previous output. Any_r signal is the ORing of all the inputs.

This design of IRRA reduces the delay and power consumption of the previous design.

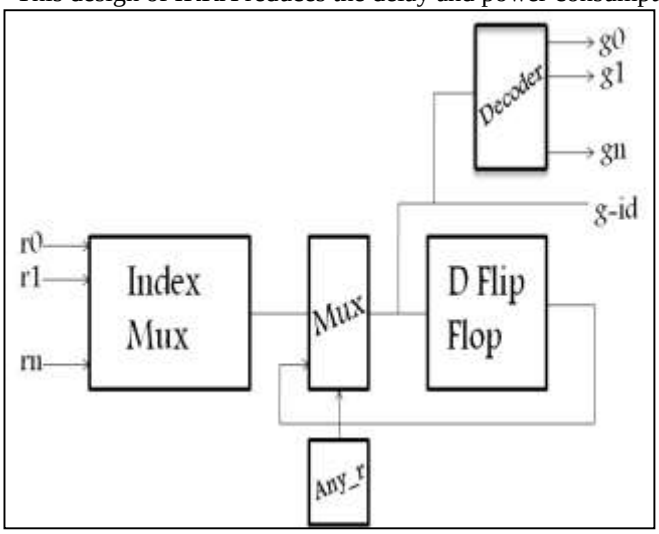


Fig. 6: Block diagram of proposed IRRA

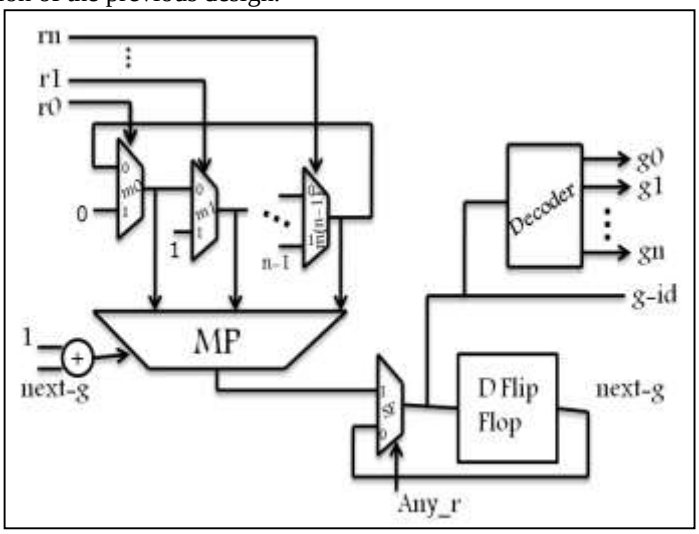
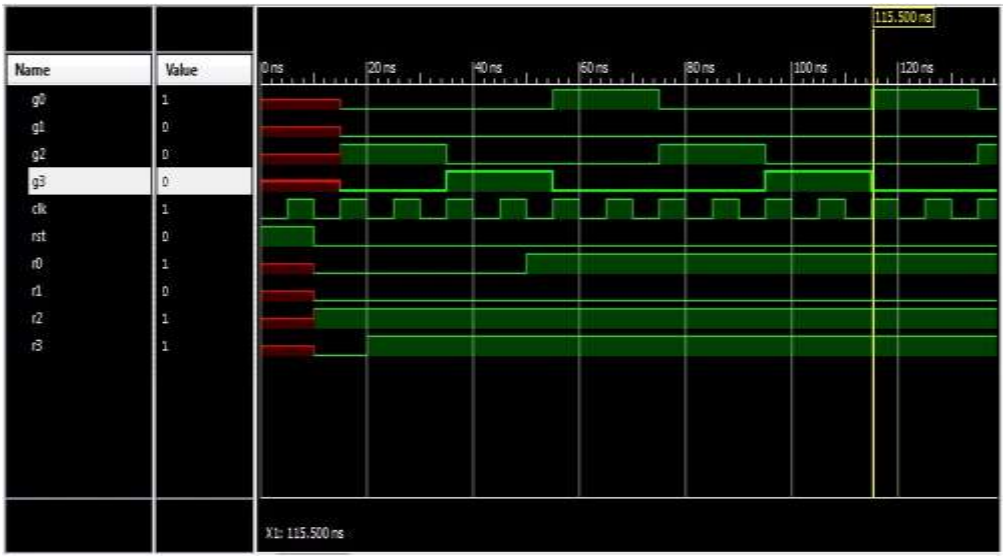


Fig. 7: Circuit diagram of proposed IRRA

V. RESULTS

Following are the obtained results of proposed IRRA and comparison table

A. Simulation result



B. Comparison table

DESIGN	*DELAY*	*POWER CONSUMPTION*	*MAXIMUM FREQUENCY*	*NO OF REGISTER*	*NO OF LUT*
PRRA	*1.633ns*	*0.042W*	*612.276MHz*	*4*	*8*
HDRA	*2.386ns*	*0.040W*	*419.182MHz*	*4*	*12*
IRRA	*1.562ns*	*0.039W*	*640.266MHz*	*4*	*11*

VI. CONCLUSION

We have presented an Index based round robin arbiter for Network-on-chip (NOC) router in FPGA design. We proved that our proposed design achieves a strong and well defined arbitration for a 4 input pattern and compared with some other previous designs such as Parallel round robin arbiter (PRRA) and High speed and decentralized round robin arbiter (HDRA) for delay and power consumption. There is a 4.34% of delay and power consumption improvement with PRRA and 34.53% of delay and power consumption improvement with HDRA. The main difference of our proposed method is its index format of the input ports. The index based round robin arbiter is simple in architecture, fast with less number of hardware components and it consumes less power as on with previous designs.

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REFERENCE

[1] V.Soteriou, R.S. Ramanujam, B. Lin, Li-Shiuan Peh. A High-Throughput Distributed Shared-Buffer NoC Router. IEEE Computer Architecture Letters, vol. 8, no. 1, pp. 21-24, Jan.-June 2009, doi:10.1109/LCA. 2009.5.
[2] Yun-Lung Lee, Jer Min Jou, and Yen-Yu Chen, "A High-Speed and Decentralized Arbiter Design for NoC," Proc. IEEE/ACS Int. Conf. on Computer Systems and Applications, Rabat,2009 pp. 350-353.
[3] Z. Fu and Xiang Ling, "The design and implementation of arbiters for Network-on-chips," Proc. 2nd Int. Conf. Industrial and Information Systems, Dalian, 2010 pp. 292-295.
[4] G. Xiaopeng, Z. Zhe, and L. Xiang, "Round robin arbiters for virtual channel router," in Computational Engineering in Systems Applications, IMACS Multiconference on, vol. 2, Oct. 2006, pp. 1610–18614.
[5] IPRRA for high speed, low power Noc router, Vikrant A. Bute1, Devendra S. Chaudhari2, (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 5 (3), 2014.
[6] The Behavior of Round Robin Arbiter in NOC Architecture, Suyog K. Dahule, Reetesh V. Golhar, Mangesh D. Ramteke, International Journal of Engineering and Innovative Technology (IJEIT) Volume 3, Issue 5, November 2013.
[7] W. J. Dally and B. Towles. "Arbitration," In: Principles and Practices of Interconnection Networks. Morgan Kaufmann Publishers, 2004, pp. 349-362.
[8] S. Q. Zheng and Mei Yang, "Algorithm-Hardware Codesign of Fast Parallel Round-Robin Arbiters", IEEE Trans Parallel and Distributed Systems, vol. 18, January 2007, pp. 84-95.
[9] S. S. Mehra, R. Kalsen and R. Sharma, "FPGA based Network-on- Chip Designing Aspects" National Conference on Advanced Computing and Communication Technology, ACCT-10, 828.
[10] Ville Rantala, Teijo Lehtonen, Juha Plosila,"Network on Chip Routing Algorithms", TUCS Technical Report, No.779, August 2006.