

# FPGA Implementation of FFT using Heterogeneous Adder

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## Abstract

In digital signal processing Fast Fourier Transform (FFT) algorithm is one of the most widely used block. The adders which plays an important role in Fast Fourier Transform (FFT). To obtain optimized Adder design in terms of delay and area many researchers have been carried out. Here, we proposed adder called heterogeneous adder which is the combination of different sub adders like ripple carry adder, carry look ahead adder, carry select adder which not only reduces delay and area but also increases the speed. These heterogeneous adders are used to design Fast Fourier Transform (FFT) architecture instead of conventional adders. In this, we have proved that Fast Fourier Transform (FFT) with heterogeneous adder gives better performance in terms of delay, area with increase in speed compared to Fast Fourier Transform (FFT) with homogeneous adder that is conventional adder. The Fast Fourier Transform (FFT) with heterogeneous adder is coded in VHDL language. Simulation is done on XILINX 14.5i tool, implemented on SPARTAN-6 kit. Overall delay and area are reduced with increase in speed.

**Keywords: Fourier Transform (FFT), Ripple Carry Adder, Carry look ahead Adder, Carry Select Adder, Heterogeneous Adder, VHDL**

## I. INTRODUCTION

The Fast Fourier Transform algorithm is discovered to make full use of hardware resources. The FFT discover is started from a period when the people started working on calculators and computers specifically we can say that to perform specific arithmetic operations. The computers and calculators are used by the Engineers, scientists and accountants to solve complex arithmetic problems and also to save the effort along with time. The basic principle of this FFT is that to find mechanism of time saving. The fast Fourier Transform analysis is to convert the original signal to a frequency domain signal and vice versa. FFT which involves the mathematics such as multiplier, adders and subtractions. For Fourier transform analysis the discrete Fourier transform(DFT) is used. The sequence of discrete Fourier transform or its inverse is computed by fast Fourier transform. And also which transforms the time domain signal to frequency domain signal.

We need to perform  $N$  multiplications and  $N-1$  additions for an  $N$ -point DFT. Therefore, there will be  $N^2$  complex multiplications and  $N(N-1)$  complex additions. Different platforms such as computer chips and general purpose processors are implemented by the Fast Fourier Transform (FFT). The FFT procedure for synthesizing and analyzing the Fourier series was given by Cooley and Tukey. And also FFT uses a divide and conquer methodology for its computation purpose. This divides the  $N$  co-efficient into smaller blocks in different stages. To calculate the Discrete Fourier Transform (DFT) the Fast Fourier Transform is the efficient way

## II. BASIC CONCEPT OF ADDERS

### A. Ripple Carry Adder (RCA):

Ripple Carry Adders are simple and more compact digital adders to generate sum of two binary numbers. These are constructed by connecting the full adders in serial manner that is previous full adder carry is connected to the next stage as a input. Full adders are the building blocks of Ripple carry adder. Hence to design  $N$ -bit parallel adders requires  $N$ -bit full adders. Here for next stage the previous stage of each carry bit ripples hence it is called as Ripple Carry Adder. It is Simple and delay is more because it must wait for the each bit of carry that is calculated by the previous adder. These adders are preferred for applications which requires a low power and reduced area.

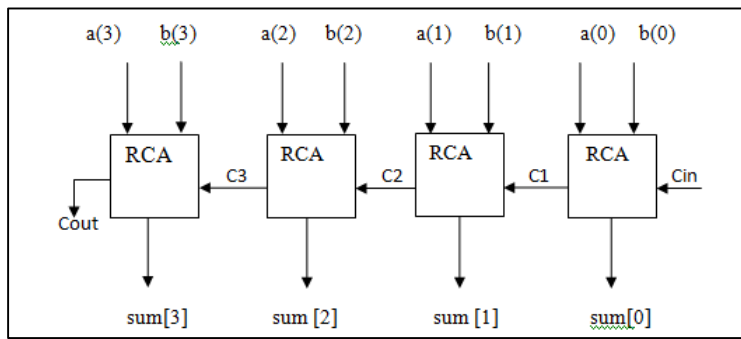


Fig. 1: Block diagram of Ripple Carry Adder

**B. Carry Look Ahead Adder (CLA):**

It is called as fast adder. Here it does not wait for the carry. The carry is generated in advance based on the input signals. Because of this the delay is reduced and performs the addition operation very quickly. The carry look ahead adder improves the speed of the adder by reducing time required for the carry propagation. But it consumes more area compared to ripple carry adder. Kogge-Stone Adder and Brent Kung Adder are the examples for this adder.

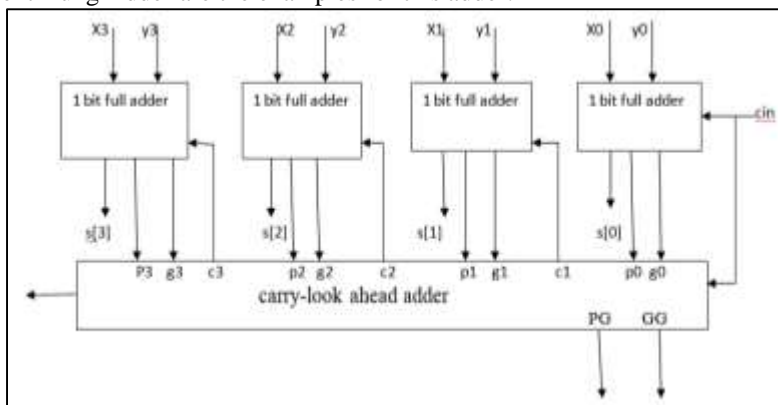


Fig. 2: Block diagram of 4-bit Carry-look ahead adder

**C. Carry Select Adder (CSA):**

The Carry select adder (CSA) architecture which consists of independent generation of sum and carry the is  $c_{in}=1$  and  $c_{in}=0$  are executed parallel. Depending upon the  $c_{in}$  the external multiplexers select the carry to be propagated to next stage. Further based on the carry input the sum will be selected. Hence the delay is reduced. However, the area of architecture is increased due to the complexity of multiplexers and two adders for each bit.

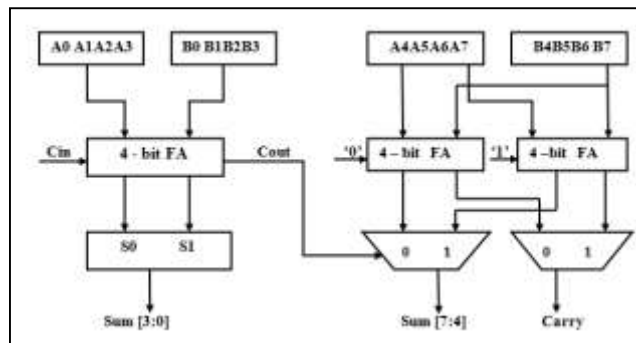


Fig. 3: Block Diagram of Carry Select Adder

**III. PROPOSED METHOD**

**A. FFT with Proposed Heterogeneous Adder:**

Butterfly diagram of Radix-2 FFT is shown in fig(a) which is called as first stage of 8-point of FFT. Where  $x(0)$ ,  $x(1)$  and  $X1$ ,  $X2$  are the inputs and outputs of FFT respectively. The output  $X1$  is obtained by adding input  $x(0)$  to the multiplication of twiddle factor and another input  $x(1)$ . Similarly output  $X2$  is obtained by adding input  $x(1)$  and multiplication of twiddle factor

along with compliment unit (-1) and input  $x(0)$ . Where the addition operation is performed by using proposed heterogeneous adder.

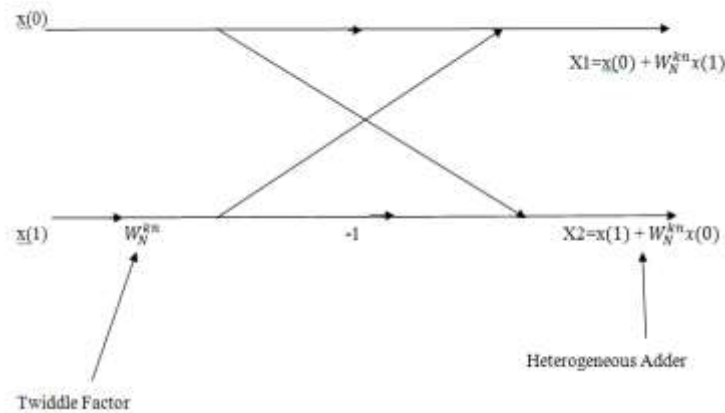


Fig 4: Butterfly diagram of Radix-2 FFT

Block diagram of Radix-2 FFT using heterogeneous adder shown in fig(b) which consists of 4 blocks such as multiplier, compliment unit and two heterogeneous adder.

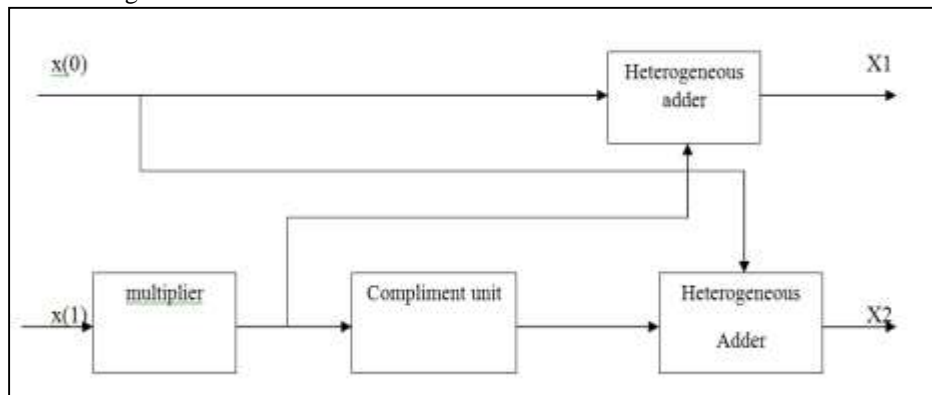


Fig 5: Block Diagram of Radix-2 FFT using Heterogeneous Adder

**B. Proposed Heterogeneous Adder:**

As there is more focus on the speed of operations in signal processing applications like fast Fourier transform (FFT) still research is there in this area. In the FFT computation both complex additions and complex multiplications are included. One of the ideas to improve the computation speed of FFT is by using the less delay adders in place of normal adders. By using a combination of different adders, the delay can be reduced with the proper selection of combination and the sequence of adders. Here for hetero adder 16 bit a combination of 4 bit two adders and 8 bit one adder are used. They are Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) and Carry Select Adder (CSA). Each of the adders have some advantages and disadvantages like some will have less delay due no carry propagation and some will have more area for the implementation.

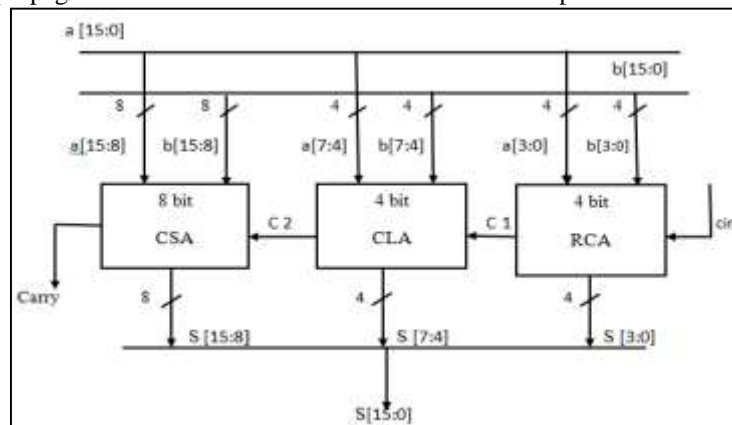
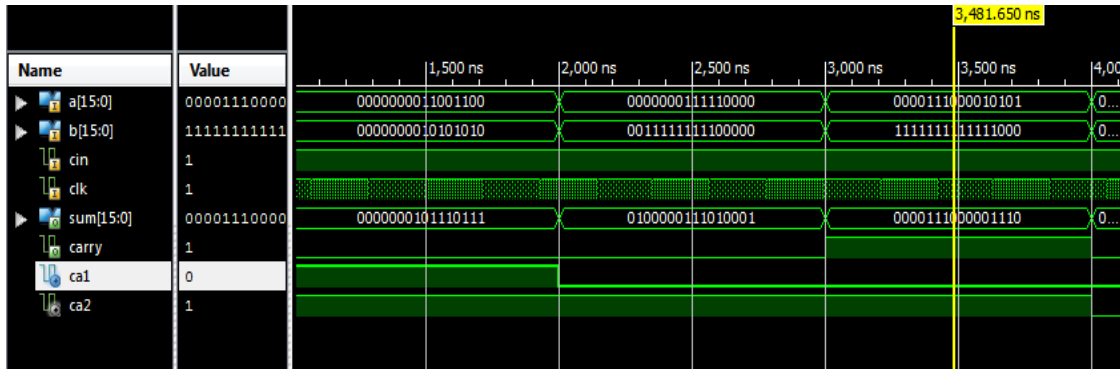


Fig 6: Proposed 16-bit Heterogeneous Adder

#### IV. RESULTS

The simulation result of 16-bit heterogeneous adder is shown below

##### A. Simulation Result:



##### B. Comparison of Adder:

Adder Type	Resolution	No. of LUTs	Delay (ns)
Carry Select Adder (Homogeneous)	16 bit	42	12.440
Proposed Heterogeneous Adder	16 bit	19	10.856

##### C. Comparison of FFT:

Parameters	FFT Using Homogeneous Adder	FFT Using Heterogeneous Adder
Number of Slice LUT's	1170 out of 27288	572 out of 27288
Delay	39.062 ns	29.864 ns

#### V. CONCLUSION

In this project the efficient implementation of FFT using heterogeneous adders is proposed. The delay of proposed heterogeneous adder is approximately 24% lesser when compared to homogeneous carry select adder. And also the area performance of the heterogeneous adders is better comparable with of the carry select adder. The Fast Fourier Transform(FFT) with heterogeneous adder is implemented by VHDL language. Simulation is done by XILINX 14.5i tool with SPARTAN-6 kit. Overall delay and area are reduced. In future, the different combination of adders can be improved for better results in synchronization with FFT Architecture.

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