Study of Reversible Logic Gates and their Designs

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Abstract

Reversible circuits that conserve information, has high-performance, release less amount of heat and it also improves the performance of the system; by uncomputing bits instead of deleting them, thus to improve the performance of the system this technique can be applied as physically possible way. Reversible logic design is also useful in improving energy efficiency. Since in new technology the main parameters to be focused on are speed power consumption and temperature; the Reversible logic can get a very important role in new technologies. Reversible computing also play vital role in portability of devices; it will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored In day today's world, as the technology is developing so rapidly the designing of the systems are becoming more and more compact. In some systems even if the circuits are not compact; still there is a need of less power consumption.

Keywords: Reversible gates, Reversible Adder, flip-flops, Reversible ALU, Reversible Logic

I. INTRODUCTION

The conventional ways of designing digital circuits were to use basic logic gates as the design entity. These gates were the foremost reason for heat generation as; bit loss during the operation of the circuit causes the energy loss. The information loss was the source of energy loss this is due to the correspondence to the number of bits decline during the working of the digital system. The total entropy of the digital system reduces after the operation due to the low density of output lines as compared to the input lines. The huge demand of portable consumer electronics products lead to the demand of designing low power VLSI circuits.

A. Reversible Gates

In a reversible logic gate a unique input is associated with a unique output and vice versa. When reversible gates operate; they never erase any information, and consequently, a computation based on reversible logic can be run forward to obtain an answer, the answer copied, and then the whole computation undone to recover all the energy expended apart from the small amount used to copy the answer at the mid-way point.

Reversible logic synthesis is the basics of quantum computing. According to the reversible networks, no fan-out and feedback constraint condition and limitation available in them, reversible logic synthesis is to implement the relevant reversible logic network also to reduce the cost as low as possible. One of the key aspects of the reversible logic synthesis is reversible logic gate cascade. In Reversible logic gate network the number of input signal/vectors are equal to output signal/vectors are one to one mapping reversible logic gate collection. Therefore, in the following way the input vectors state can be described: if every input vectors of function can only be mapped by only one output vector then it can be said that the function is reversible. Therefore, the input vectors state can only be reconstructed by the output vectors, which are described by the way of the function as following: the function is reversible, if every input vectors of function can only be mapped by only one output vector.

B. Peres Gates

Fig.1 shows the block diagram of Peres Gate. It three inputs A, B and C and three outputs P = A, Q = A XOR B and R = AB XOR C. Its quantum cost is 4.

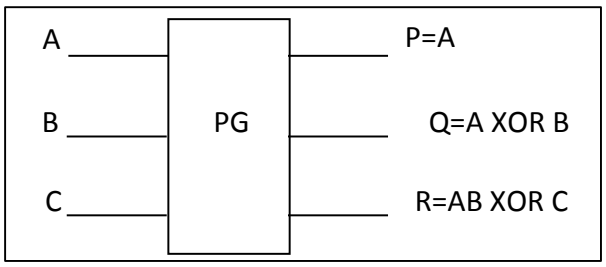

Fig. 1: Peres Gate

C. *Feynman Gate*

Fig.2 shows the block diagram of Feynman Gate, it is also called as Controlled-Not (CNOT) gate. Its quantum cost is 1. FG has two inputs as A and B and the two outputs as P = A and Q = A xor B.

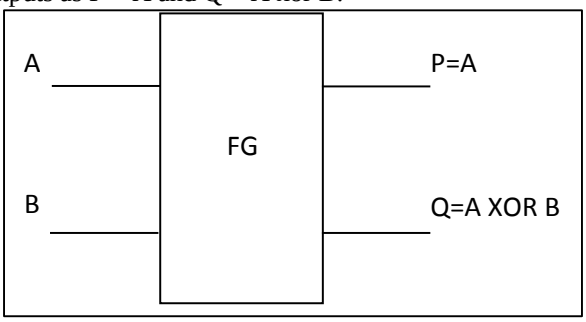

Fig. 2: Feynmen Gate

D. *Toffoli Gate*

Toffoli gate given in Fig 1, the first (n-l) bits are called as control lines and last bit is called as target line. The target bit is toggled only when all control lines are 1. The Toffoli gate has Quantum cost of 5 n number of inputs and outputs.

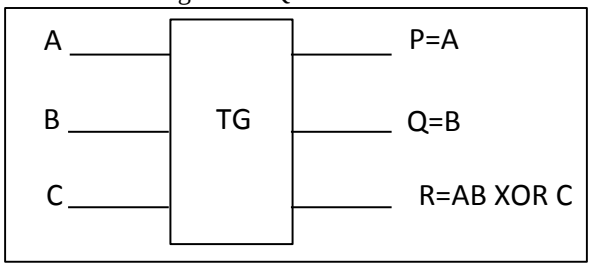

Fig. 3: Toffoli Gate

E. *NSG Gate*

A 4 * 4 one through reversible gate called NS gate "NSG" is projected. The reversible NSG gate is given in Figure4. The matter of fact that invented gate can utilize as NAND and NOR operation that refer that any Boolean function can be implemented using this gate NAND and NOR is universal gate.

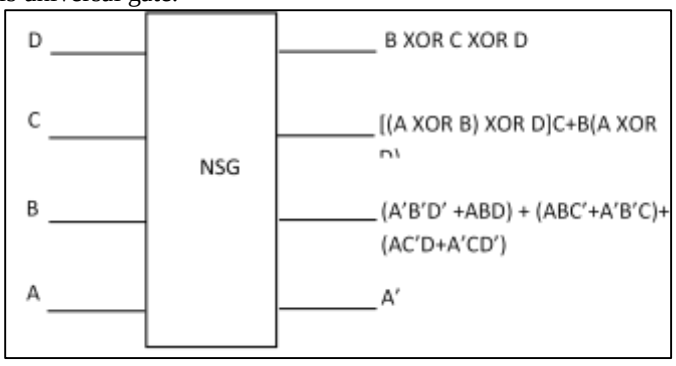

Fig. 3: NS Gate

Thus by using such reversible gates we can make any system with low power and higher efficiency. In this paper some of the applications are given just to make sure that there is the possibility that any design or system can be made using reversible logic gates.

II. LITERATURE REVIEW

K.V Manoj and M.Amarnath Reddy [1] in there paper they presents the primitive reversible gates that are gathered from the references and made the adder as an application of Reversible gates. Their paper led to extend towards the digital style development mistreatment reversible logic circuits with pass junction transistor logic which helps to form an occasional power circuits.

P.Vanusha, K.Amurtha Vally [2] in their paper showed the implement some of the reversible logic gates and their applications and their simulation using Tanner EDA software. They also stated that reversible logic circuits play a very important role in design of low power digital circuits of a future computer. low power CMOS design.

Matthew Morrison and Nagarajan Ranganathan [3] concluded the new ALU designs which are advantageous to previously published work in implementations that favor low delay and high logical calculation output, which is desirable for realization of a reversible central processing unit. They proposed MRG and PAOG matched the HNG as the best existing 4*4 reversible gates in terms of cost, delay and logical output calculations.

K. Prasad Babu, S. Ahmed Basha, M. Chennaiah, H.Devanna. They concluded that the Power dissipation of Full adder circuit is low. Thus they said that of the three reversible gates used (NG,NTG,NG+NTG) for design of Full Adder reversible NTG gates uses low power. In Future with voltage scaling much reduction in power can be achieved.

III. FLIPFLOPS USING REVERSIBLE GATES

Fig shown below is of toggle flipflop using Fredkin and feynman reversible gates. It uses 2 fredkin and 3 feynman gates.

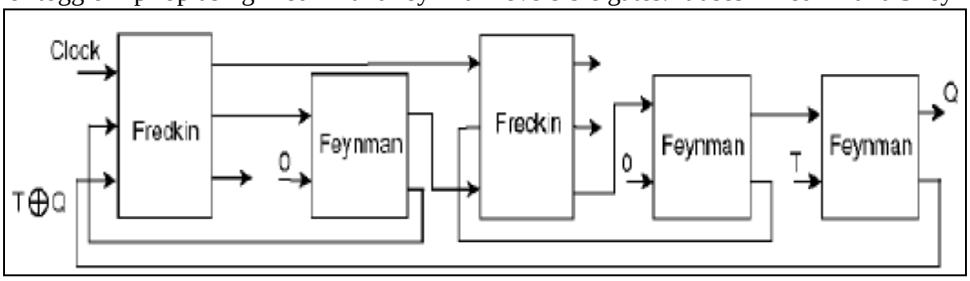

Fig. 5: Flip-Flops using Reversible gates

A. Full Adder using Reversible Gates

Fig 6shows the scheamatic for Full adder using NG Gate and NT Gate. The A XOR B is the garbage Value and not considered in the equation.

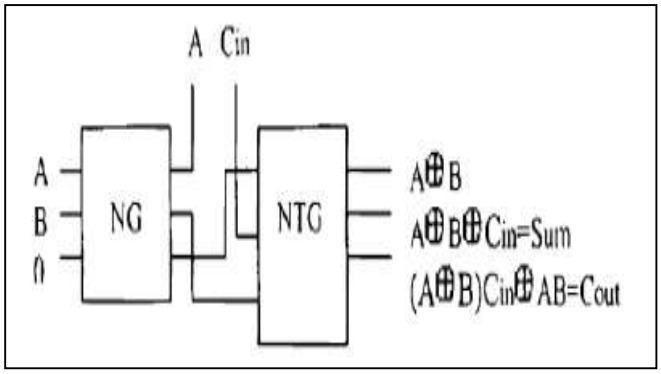

Fig. 6: Full Adder Using Reversible Gates

B. Arithmetic Logic Unit using Reversible Gates

The Arithmetic Logic Unit which is the most important part of computing can also designed using Reversible gates; the combination of multiple reversible gates results into successful and power efficient ALU as shown in fig7.

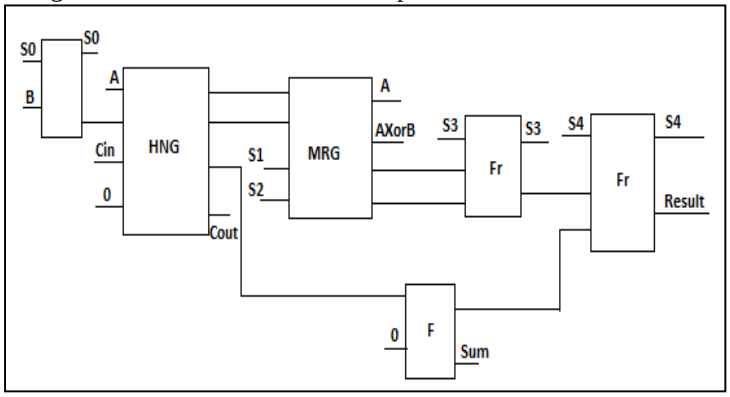

Fig. 7: Reversible ALU

IV. APPLICATIONS

Reversible computing can be applicable in various recent technologies where there is need of very Low power, higher transmission rates, fast processing's, long term beneficial systems and reducing the cost.
Some of the areas of the application of Reversible designs can be listed as follows:

1) Low power CMOS.
2) Quantum computing Technology.
3) Nanotechnology
4) Design for Low Power Digital Signal Processing(DSP)
5) Extremely low power Field Programmable Gate Arrays (FPGAs) in CMOS technology, self-repairing designs And lots more.

V. CONCLUSION

The reversible logic circuits play a very important role in design of low power digital circuits of a future computer. This has led many researchers design circuits related to advanced computing, low power CMOS design. In this paper led to implement some of the reversible logic gates and their applications.

From the above proposed plan it can be concluded that the reversible gates can be used to design any type of combinational circuits. Such type of circuits will be helpful to achieve less delay, and also reduced number of gates. It might be possible that the area of design will increase but; the main thing in present technology is to reduce the power which will definitely work using such gates. The various designed application clears that there can be various other gates which can be combined to design even sequential circuits. This also makes one conclusion that all the older systems can be made compatible with the emerging as well as future technology.

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