A Power Analysis of SRAM Cell using 12T Topology for Faster Data Transmission

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Abstract

High Power Consumption Rate of the Chips is one on the major problems faced by the circuit designers in today’s world. This paper represents an improved 12T Static Random Access Memory (SRAM) cell with the following advantages – reduced leakage current and enhanced performance, by using 180NM Technology. The SRAM cell is the need of high speed digital computing system. The switching of the transistors and leakage current during the off state of device results in more power consumption in the digital cell. To compare the proposed work with existing structure available with 12T, the proposed design gives the following advantages: reduction in the power consumption and increase in the data transmission speed. The design layout of the simulation will be carried on the Tanner tools 0.18um CMOS technology.

Keywords: SRAM Cell, CMOS, leakage current, power, 12T SRAM Cell, read, write

I. INTRODUCTION

The SRAM cell is the main memory device used in modern digital system. Memory is referring as to the computer hardware device used to store information. There are two types of memory as follows

1) Static random access memory (SRAM)
2) Dynamic random access memory (DRAM)

A Static random access memory is a semiconductor memory used to store each bit. It is called as volatile memory because it depends upon the constant voltage supply, to hold the stored data. But in Nonvolatile random access memory they save the data when power supply is lost. SRAM is independent on constant refresh cycle.

B) Dynamic random access memory cell requires a capacitor to store the data in the cell. DRAM requires a constant refresh cycle at all time to maintain the store data as it is in the cell. So that it consumes more power as compare to SRAM cell.

SRAM cell is faster cell but it has large leakage current so that power consumption is also increases in SRAM. So it is necessary to design a SRAM cell with a low leakage current and reduced power circuit. There are many ways to reduce power consumption such as by reducing power supply also by using stack effect and clock gating technique. So that first is necessary to reduce the threshold voltage to maintain high drive current and increase the performance of cell. For the reduction of power dissipation and increase the performance we analyze the 12T SRAM cell.

II. LITERATURE REVIEW

Jaydeep P. Kulkarni [1]. The proposed shows ultra-voltage operation of different SRAM cell is explained. The ultra-voltage operation is performed by lowering the supply voltage. The proposed ST-2-bit cell gives 1.6 times higher read static margin and 2 times write static margin as compare to 6T SRAM. For achieving low voltage operation 6T/8T/10T/ST SRAM topologies are studied in this paper. Results are carried out at 130nm technology, which give the effectiveness of proposed bit cell for successive ultra-low voltage operation.

Mohsen Imani, Haleh Alimohamadi [2] proposed low power 12T SRAM cell with 16nm at 800mv supply voltage CMOS technology. The proposed 12T SRAM cell is compared with the 9T and 10T SRAM cell which shows that the leakage current is reduced by using two stack transistors at read path. The reliability of cell also increases by increasing read SNM. The proposed cell has 5.5% and 27.4% higher read SNM from 9T and 10T respectively. The power consumption of proposed 12T cell has lowered by 35.5% and 43.8% as comparison of 9T cell and 10T cell.

Ambrish Mall, Suryabhan Pratap Singh, Manish Mishra, Geetika Shrivastava [3], states that this paper gives the brief development in low power circuit. In standby mode the power consumption is more. The proposed circuit contains a series connected tail transistor which turn down the leakage current which results in, low power consumption of cell. The proposed 12T SRAM cell is compared with low power 10T SRAM cell on 45nm and 32nm technology, it gives the power reduced by 45.94% (0.4v) and 31.08% (0.3v) respectively.

K.G.Dharani [4], this paper gives the comparative analysis of 6T, 8T and 12T SRAM memory cell by power, layout and current values of the cell. In 6T, 8T, 12T the current values may be change during read and write operation but the power consumption is
increased in 12T. But 12 T has a high capability to hold the data in the memory. This paper specifies that 6T has very less read margin with 8T transistor however 8T has high write noise margin.

Mekala Tajeswar, P. Brundavani[5], in this paper, the operation of 12T SRAM cell on multi threshold CMOS technology are studied. This paper gives the reduction in power consumption of SRAM cell by adding transmission gate. By applying two sleep transistors the leakage current during hold mode is reduced and by applying two voltages at the output swing voltage is reduced. On the basis of power consumption, the proposed 12T SRAM cell is compared with the 6T SRAM cell, which shows that the power dissipation in 6T SRAM is 0.182mw and power dissipation at 12T SRAM is 0.169mw. Proposed clearly indicates 12T SRAM gives the better performance and high speed data transmission with or without recovery boosting technique.

M.Gangasukanya, P.Asiya Thapaswin[6], this paper introduced a 12T SRAM with high data transmission speed at 45nm technology and low power consumption. In this paper, proposed 12T SRAM cell is studied at different temperature. The proposed SRAM cell has two high voltage sleep transistor and a low Voltage transistor to minimize the power consumption during changing of mode from hold to active mode, so that the static power is also reduced in the cell. By applying two voltages at the output the dynamic power is reduced in this paper. The first voltage is applied to the bit line and second voltage is applied to the bit line bar, which overcomes the swing voltage so that the swing in swing voltage there in reduction in leakage current also during hold mode this technique the power consumption of SRAM cell is reduced.

P.Pavan Kumar, Dr. R Ramana Reddy, M.LakshPrasanna Rani[7], this paper introduced the 4T SRAM with low power consumption. The proposed 4T SRAM is compared basic structure of 4T SRAM. The software used for this project was mentor graphics at 130nm technology. The NMOS and inverter were used to design the proposed 4T SRAM. The static power is reduced by 41%, delay is reduced by 36%, total power is reduced by 32% and occupies 32.46% less area as compare to conventional 4T SRAM cell.

III. DESIGN OF 4T SRAM CELL

The SRAM Cell is designed so as to have proper read operation and reliable write operation. Fig. 3 shows the structure of 4T SRAM cell.

SRAM cell uses two P-type metal-oxide semiconductor (PMOS), two N-type metal-oxide-semiconductor (NMOS) and load register. The load registers used are made up of either poly silicon or depletion type of NMOS or PMOS.

There are three modes in which the SRAM operates:
1) Standby mode: In this mode, word line is not asserted. So that the pass transistor is deactivate. So that no read and writes operation is performed in this mode and ram hold the stored data. The power required for holding the data is more.
2) Read mode: Read operation is performed by first activate the word line and the pass transistor are activated. The voltage at bit line (B) is kept high and the bit bar line (Bbar) is pulled to low. When the difference between two voltages is detected as high, that time 1 is read. When the difference between them is minimum, it means 0 is read from the cell.
3) Write mode: When 1 has to write in to the cell that time first have to make bit line high and bit bar line at low voltage. Similarly, when 0 has to write in to the cell then bit line (B) is kept at low and bit line bar (Bbar) is at high voltage.

IV. DESIGN OF 6T SRAM CELL

The circuit for 6T SRAM cell is symmetrical in nature. The circuit of 6T is as shown in figure 4.

The circuit is built with two pmos and four nmos. M2 transistor is connected to the bit line(B) and bit line bar (Bbar) is connected to transistor M1. Bit line and bit line bar is used to data to be written in to the cell. And word line is use for read and write operation. Q and Qbar are used as the storing nodes. When node Q stores 0, the node Qbar stores 1. In such case transistor N4 and P2 are turned on. Same time transistor P1 and N4 turned off.

When word line is not selected (in hold mode) at that time pass transistor M2 and M1 are off and circuit is on idle mode (hold mode). When data is to write in the cell, first data has to give to the bit line (B). Bit line bar (Bbar) has compliment of bit line data. When data 1 is to be written on cell, select the word line (WL=1) so that the transistor N1 and N2 are turn on, and bit line is also 1
and data is stored in to the cross coupled inverter. When data 0 has to written in the node storing 1, the corresponding bit line is applied with voltage 0 and bit line bar to Vdd and also word line (WL) to vdd.

![Fig. 2: 6T SRAM Cell](image)

In read operation mode, first pre-charged the bit line and bit line bar to high and turn on word line (WL). The transistor N1 and N2 are turn on. Values stored in Q and Qbar are applied to bit line. Bit line and bit line bar will be pulled down depending on Q and Q. If Q=0, Qbar=1, Bit line (BL) discharges and bit line bar keep high and vice versa.

V. DESIGN AND OPERATION OF 12T SRAM CELL

The analysis of power is studied from the paper presented by Mohsen Imani, Haleh Alimohamadi as mentioned above. Based on those results we will design the 12T SRAM in CMOS technology at 180 nm technology. The Proposed 12T SRAM cell circuit have low voltage; low power consumption and delay will be reduced. The circuit for 12 T SRAM presented by Mohsen Imani, Haleh Alimohamadi has a OR gate in the circuitry. So that it increases the power consumption of cell. The power required for Or gate is same as the power required for the 6T SRAM cell. So that that OR gate is replaced by single transistor in this proposed SRAM Cell. The power consumption of cell is mainly due to the static or dynamic power in the circuit. The dynamic power is depend on the time taken by the input signal to change the state from low level to another level in the circuit. Static power is mainly during off or holds state state or when leakage current flow through the device. To overcome the problem some average merits needed to bring the current flowing through device to zero or bypass the leakage current from off device. As the delay reduces, power will be automatically reduced. The proposed SRAM will be used in high speed application devices. As the number of transistor increases the storing capacity of SRAM is increases as well as the power consumption of cell is also increases. The main objectives of the proposed SRAM cell are to reduce the power consumption and improve the speed of data transmission by reducing the delay in the circuit.

The proposed SRAM circuit is as shown fig3. It consists of 4PMOS and 9NMOS transistor. The transistor 7 is used to control the leakage current flowing through circuit in off state or through device.

SRAM cell is operated in three modes as follows

Hold / Standby mode: In this mode, word line is not asserted. So that the pass transistor is deactivate. So that no read and writes operation is performed in this mode and ram hold the stored data. The power required for holding the data is more.

Read Mode: Read operation is performed by first activate the word line and the pass transistor is activated. The voltage at bit line (B) is kept high and the bit bar line (Bbar) is pulled to low. When the difference between two voltages is detected as high, that time 1 is read. When the difference between them is minimum, it means 0 is read from the cell. The read operation is carried out only from storage node QB. When node Q store 1 and QB sores 0 that time, transistor 9 is on and when QB stores 1 and Q stores 0, that time transistor 8 is on. The data is transferred to the pass transistor nmos1 and nmos2 and read out through them.
Write mode: when data has to written in to the cell first turn on the word line and the data is given to the bit line (BL) and bit line bar (BL\bar{1}). When 1 has to write in to the cell that time first have to make bit line high and bit bar line at low voltage. Similarly, when 0 has to write in to the cell then bit line (B) is kept at low and bit line bar (B\bar{bar}) is at high voltage.

<table>
<thead>
<tr>
<th>Cell operation nodes</th>
<th>WR</th>
<th>RD</th>
<th>HS= (WR or RD)</th>
</tr>
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<tbody>
<tr>
<td>Read</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Write</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Hold</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 1. The control signals in different operation node.

VI. SIMULATION RESULTS AND PERFORMANCE COMPARISON

Tanner Software is used for simulation of the design. In order to compare the modified 12T SRAM with the previous designed both the circuits have been simulated in a 0.18\micro m CMOS technology with VDD = 1.8V. The power of modified 12T SRAM is significantly reduced in low voltage supply.
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Fig. 5: Output Waveform of 6T SRAM cell

Fig. 6: Output Waveform of 12T SRAM cell

Table – 2
Compares the performance of modified 12T SRAM as compare to 4T, 6T SRAM

<table>
<thead>
<tr>
<th>Parameters</th>
<th>4T Technology</th>
<th>6T Technology</th>
<th>12T (existing) Technology</th>
<th>12T (proposed) Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180nm</td>
<td>180nm</td>
<td>180nm</td>
<td>180nm</td>
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<tr>
<td>Supply Voltage</td>
<td>1.8v</td>
<td>1.8v</td>
<td>1.8v</td>
<td>1.8v</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2.5nw</td>
<td>1.21uw</td>
<td>1.22uw</td>
<td>9.384nw</td>
</tr>
<tr>
<td>Delay</td>
<td>2.71ns</td>
<td>1.001ns</td>
<td>60.5ns</td>
<td>60.005ns</td>
</tr>
</tbody>
</table>

VII. APPLICATION

SRAM cell is used in personal computers, routers and peripheral equipment, workstations.
It is also used in a CPU register files, internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc

VIII. CONCLUSION

These days, in an electronic devices having very high demand for low power consumption devices. This paper introduced a 12T SRAM with low power consumption with a faster data transmission speed. Power consumption of 12T SRAM cell is higher as compare to 4T/6T. The power consumption of proposed 12T is less than the existing circuit of 12T. The proposed SRAM gives the less power consumption as well as increase the speed response of the cell.
REFERENCES

[4] K.G.Dharani,“Comparative Analysis of 6 Transistor, 8 Transistor and 12 Transistor SRAM Memories” Research Scholar, Karpagam University, Coimbatore Tamilnadu, India.

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