Implementation of RISC Microprocessor for DSP Systems

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Abstract

This paper is about the reduced instruction set computer (RISC), microprocessor CPU design that flavors a smaller and simpler set of instruction. In this project we have described 16-bit pipelined RISC processor for applications such as in real time digital signal processor and embedded systems. The processor designed specifically for DSP systems such as FFT, DWT, Convolution and ALU, executes most of instructions in a single cycle; conventional processors usually performs only arithmetic and mathematical operations. Hence RISC processors have complex control system which requires more clock cycle to operate, thus we overcome this problem using pipelined architecture of 4 stages i.e fetch, decode, execute and write back. In fact compared to base paper the area is reduced and speed is increased. The Simulation is done on XILINX 14.5i tool, implemented on SPARTAN-6 kit. Over all speed is achieved and results are verified.

Keywords: Reduced instruction set computer(RISC), Digital Signal Processor (DSP), Fast Fourier Transform(FFT), Discrete wavelet transform(DWT), VHDL

I. INTRODUCTION

It seems now overpowering case in RISC as high performance computing engines, there is a rapid acceleration of performance in current generation of CPU. The history of RISC processor which was 1st introduced since late 1980's. It was created by David Patterson of berkeley RISC project. It is CPU design based on a simplified instruction set which provides higher performance when combined with microprocessor architecture which can handle executing those instructions using fewer cycles per instruction.

The general concept is that the system uses small, highly optimized set of instruction instead of more variable set of instructions frequently found in other types of architecture. The famous RISC families include AMD, Atmel2900, MIPS, SPARC and RISCV. Complex instruction set computer (CISC) opposed trend to RISC. Where as in RISC it uses load and store instructions refer data in memory, it uses fewer addressing modes with fixed length of instruction and unique format. Main characteristics of RISC microprocessor is it needs hard-wired, instead of using micro programming and also to implement CPU takes less area, speed are increased. As known RISC was used to perform ALU operations generally, so to use for custom design i.e for different DSP applications this can be achieved using RISC Processor. In this project we are using pipelined architecture.

In present era the development of CMOS technology yields very high density and high performance integrated circuits. This estimates that as increasing devices on chip which as well increases the overall performance of device but it has disadvantage of power consumption also becomes serious terrifying issue along with complexity of circuits. Hence, it becomes inevitable to implement less complex, low power processors. In this work combination of RISC and DSP is done to improve speed of processor.

II. BASIC CONCEPT OF PROCESSOR

A. *Basic Block Diagram of RISC:*

When designing processor, mainly consider frequency of operation. The frequency target determines how many gates of logic can be included per pipeline stage. Memory and bus architecture design of dsp is guided by optimization of speed and focuses on throughput. Instruction fetch the necessary data are drawn from memory, opcode is received in the decoder. Value of each instruction is 32 bit in length.

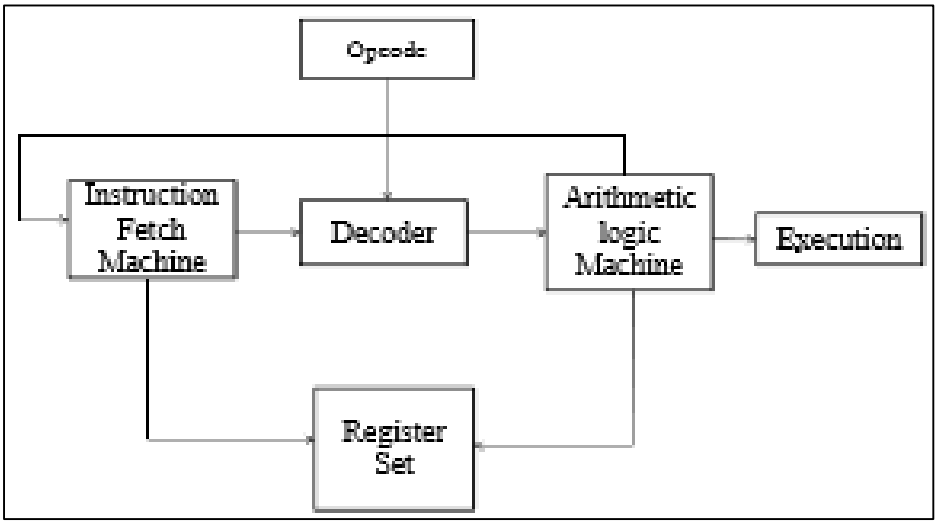

Fig. 1: Basic block diagram

Here design is of 4 stages which consist of:

1) Fetch
2) Decode
3) Execute
4) Write back

Inst r No.	Pipeline Stage						
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX
Clock Cycle	1	2	3	4	5	6	7

Fig. 2: Pipeline stages

1) Fetch: on every positive clock cycle of input, the fetch stage increments the value of counter which initially is set to zero during processor bring up. The value of counter is used to fetch the instructions that are stored in memory.
2) Decode :decode stage is second cycle of pipeline where the instruction is fetched from instruction memory is decoded to different signals based on signal which is fed to execute stage for execution of instruction. Input to decode is 16 bit instruction that is fetched from fetch stage.
3) Execute stage: it receives the output from decode stage and it performs execution of the instruction. The execute stage performs various operations like add, subtract, increment, decrement, logical operations, and DSP operations.
4) Write back stage: it stores the output of execute stage in a register. The value could be either from ALU or data memory, depending on register load/Store instruction, the multiplexer in write back stage gets the values register address or indirect addressing is used. This address is then input to data memory which in turn fetches correct data from the index provided by output.

III. PROPOSED METHOD

The design of RISC microprocessor for DSP system is shown below, it is designed using the decoder block, opcode, controller, data memory, and Instruction set. We have designed for DSP applications such as convolution, FFT, DWT and ALU operations can be performed using this design. The technique used is pipeline architecture i.e it takes any data as input by passing one block.

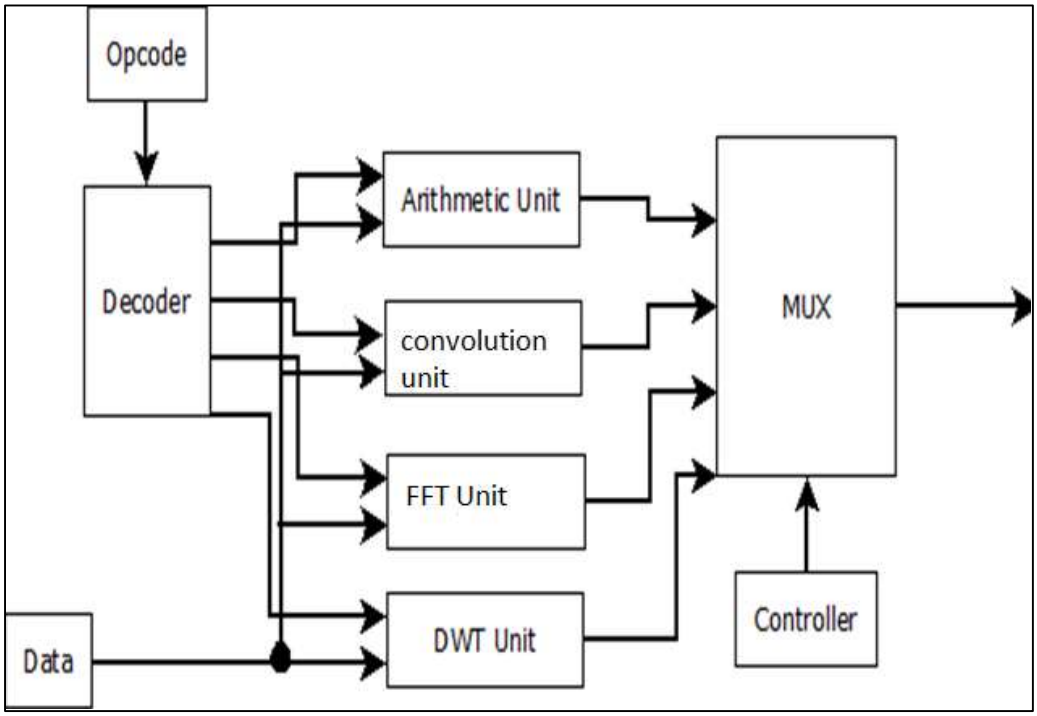

Fig. 3: Proposed block diagram

1) ALU: Performs all arithmetic and logical operations, which is designed using different adders and MAC unit.
2) Convolution: Is a simple mathematical operation which is fundamental to many common image processing operators. It provides a way of multiplying the two arrays of numbers, whose size is different. And this operation is done using Gaussian filter which removes noise present in image, uses 3*3 window .The image consist of 256*256 pixels.
3) Fast Fourier Transform (FFT): is the most widely used algorithm in digital signal processor, image processing etc. FFT is the concept of conversions of time domain signal to frequency domain signal and vice versa. Usually in time domain Discrete Fourier Transform is mainly used computation. By applying this DFT to digital input signal will obtain the output as a frequency domain signal.

$$\mathbf{Xk}=\sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N} \quad \mathbf{k=0\ldots N\text{-}1} \quad \ldots.$$

$$Xk = \sum_{n=0}^{N-1} \frac{x(n)cos2\pi nk}{N} - j\sum_{n=0}^{N-1} \frac{x(n)sin2\pi nk}{N}$$

4) DWT (Discrete wavelet transforms): It is flexible method for breaking of signals; here signal energy is concentrated only to particular wavelet coefficients. Here we have used HAAR wavelet. This is used for image compression applications by considering only required coefficients and neglecting extra cofactors.

IV. RESULTS

The simulation result of ALU and DSP operations are shown below

A. Simulation Results:

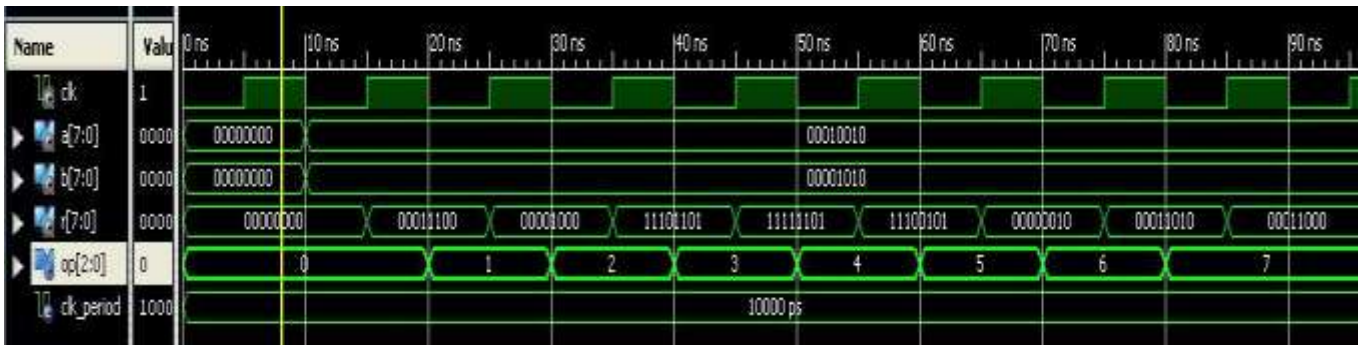

Fig. 4: simulation result of ALU operations.

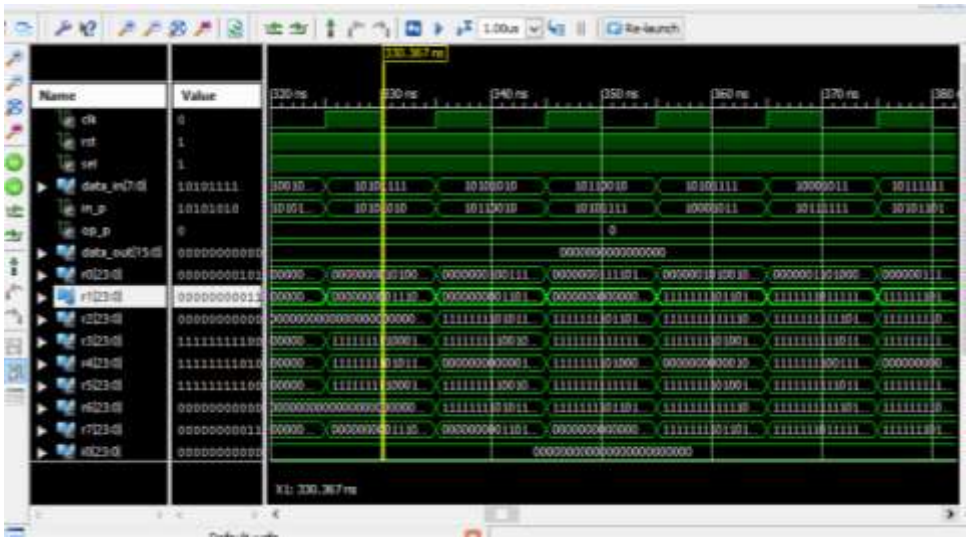

Fig. 5: Simulation result of FFT.

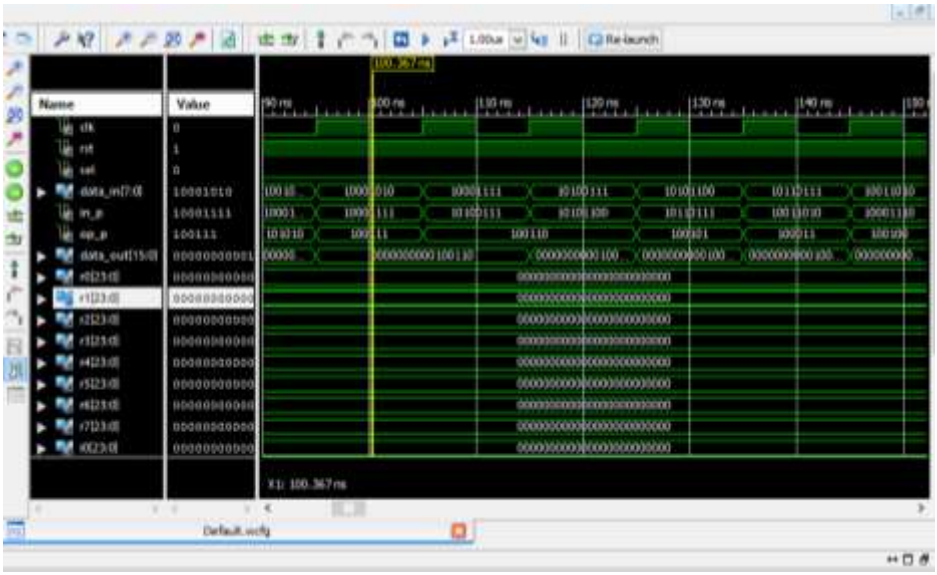

Fig. 6: Simulation result of convolution.

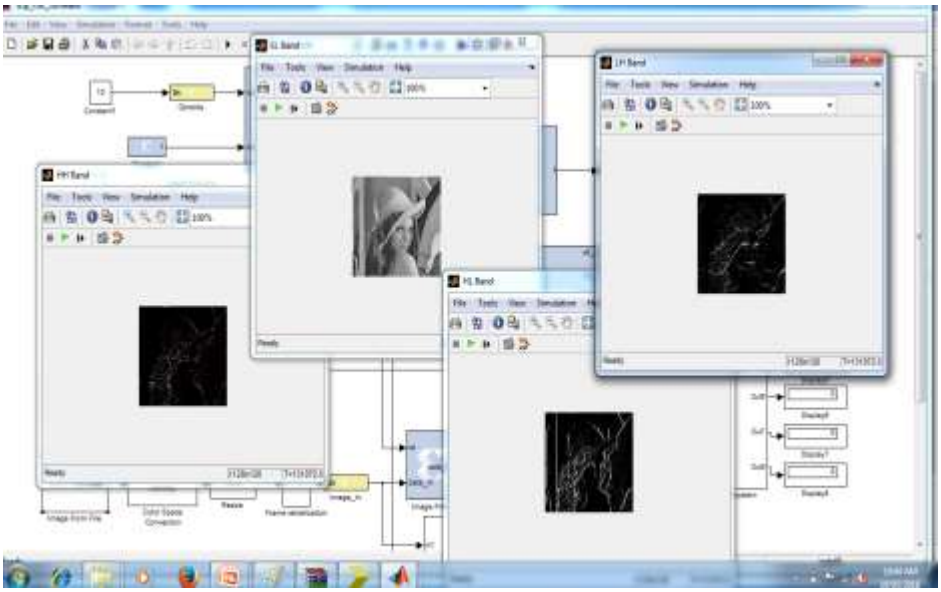

Fig. 7: Software model of dwt output

V. CONCLUSION

In this project the efficient implementation of RISC processor is done. We have designed risc processor for dsp applications and is implemented on Xilinx 14.5 using Spartan 6 FPGA kit. The simulation results indicate that area is reduced by 6% in comparison with existing paper and speed is improved .In future In Future it can be extended to implement for CISC Processor, in soc, and for medical applications. Can be implemented for superpiplined and superscalar processors.

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