Design and Synthesis of ALU using Reversible Logic for MAC Applications

Dilshadbanu M Matte
PG Student
Department of VLSI Design & Embedded Systems
Center for PG Studies, Visvesvaraya Technological University, Belagavi, Karnataka, India

Dr. Meghana Kulkarni
Associate Professor
Department of VLSI Design & Embedded Systems
Center for PG Studies, Visvesvaraya Technological University, Belagavi, Karnataka, India

Abstract

Reversible computing technique is one of the most efficient and prominent techniques used in low power circuits. In this paper design of reversible ALU is proposed for MAC applications which can be verified using Xilinx ISE 14.5 software tool. The comparison parameters are quantum cost, garbage output, number of constant inputs, number of gates used that is gate count and propagation delay.

Keywords: Proposed reversible ALU design, reversible multiplier, reversible shifter, reversible priority encoder, reversible multiplexers, reversible multiply accumulate unit

I. INTRODUCTION

Power dissipation is one of the major issues in today's technology. In the year 1960 R Landauer was demonstrated that the power dissipation is due to the loss of information in high technology circuit and system constructed using irreversible logic gates. According to Landauer's principle there is power dissipation of kTln2 joules of per bit of information loss in irreversible logic gates where k is Boltzmanns constant, T is absolute temperature. According to Bennett, to overcome with kTln2 joules of power dissipation in circuit, it must be built the circuit with reversible logic gates. Reversible logic gates having equal number of inputs and outputs that is n*n inputs and outputs and there is one-to-one mapping between input and output vectors. It helps to determine the outputs from the inputs as well as the inputs can be recovered from the outputs.

The reversible logic having the following features:

- The number of inputs and outputs must be equal.
- For each input patterns there is a different output patterns.
- Fan out is not allowed.
- One-to-one mapping between input and output vectors.

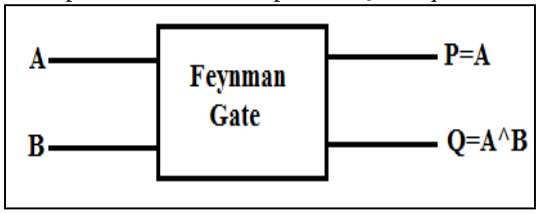
The reversible logic gates having the following features:

- Number of gates used in circuit should be minimum.
- Number of constant inputs used in the circuit should be minimum.
- Number of garbage outputs in the circuit should be minimum.
- Quantum cost of reversible logic gate is in terms of the cost of a primitive gate.

II. TYPES OF REVERSIBLE LOGIC GATES

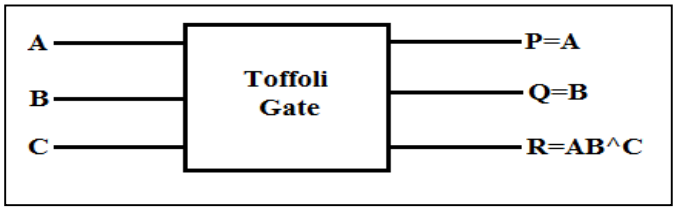
A. *Feynman Gate:*

It is 2*2 reversible gate which having the 2 inputs A, B and 2 outputs P, Q and quantum cost is 1.



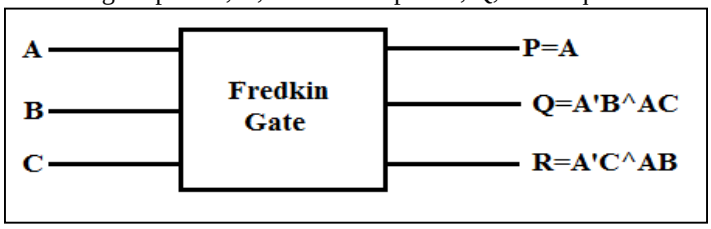
B. *Toffoli Gate:*

It is 3*3 reversible gate which having 3 inputs A, B, C and 3 outputs P, Q, R and quantum cost is 5.



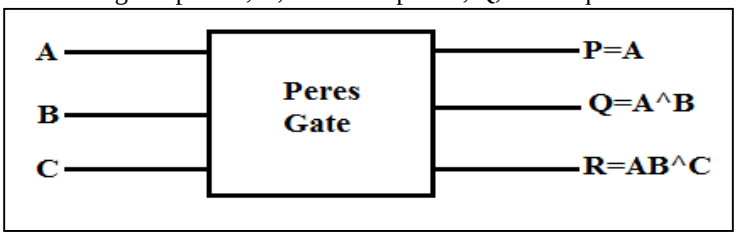
C. *Fredkin Gate:*

It is also 3*3 reversible gate which having 3inputs A, B, C and 3 outputs P, Q, R and quantum cost is 5.



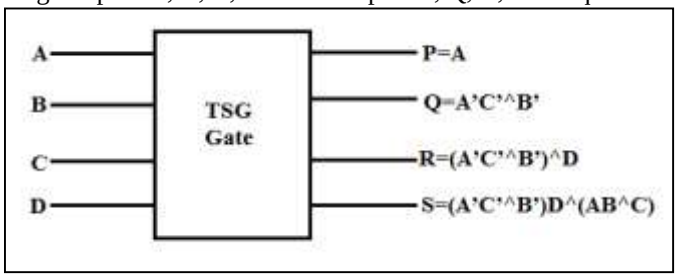
D. *Peres Gate:*

It is also 3*3 reversible gate which having 3 inputs A, B, C & 3 outputs P, Q, R and quantum cost is 4.



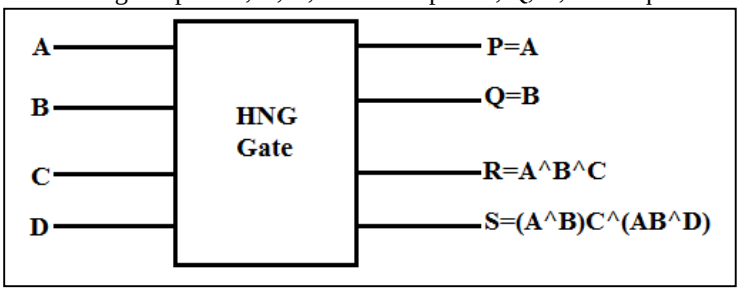
E. *TSG Gate:*

It is 4*4 reversible gate which having 4 inputs A, B, C, D and 4 outputs P, Q, R, S and quantum cost is 4.



F. *HNG Gate:*

It is also 4*4 reversible gate which having 4 inputs A, B, C, D & 4 outputs P, Q, R, S and quantum cost is 6.



III. PROPOSED METHODOLOGY

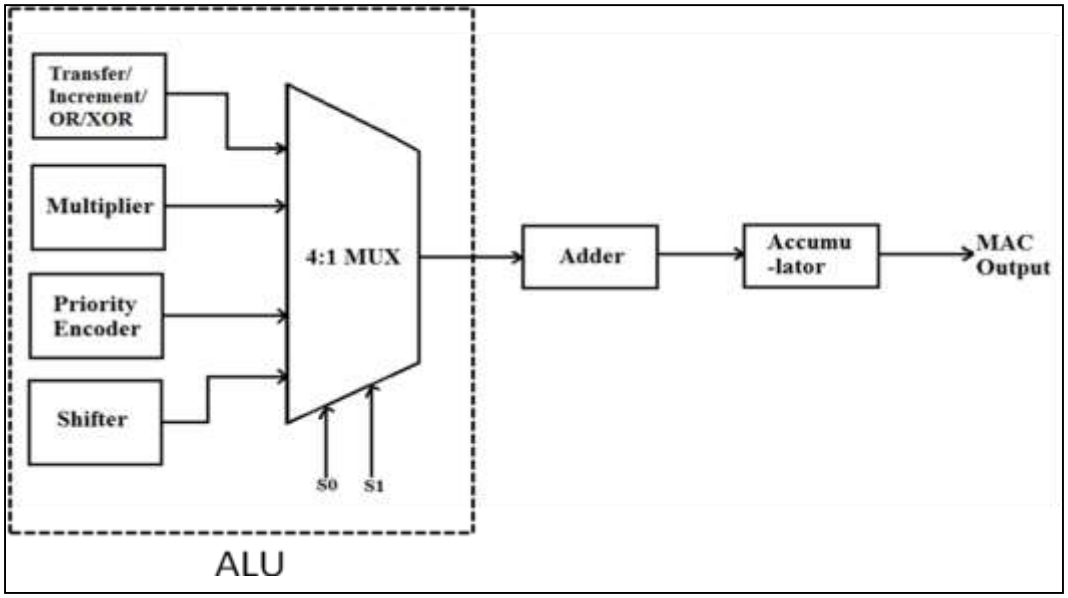


Fig. 1: Proposed block diagram of reversible ALU

The proposed reversible ALU is design using MUX as shown in figure1 which performs the arithmetic and logic operations. The first block of ALU performs 12 operations. The design consist of control unit and reversible full adder as shown in figure2.

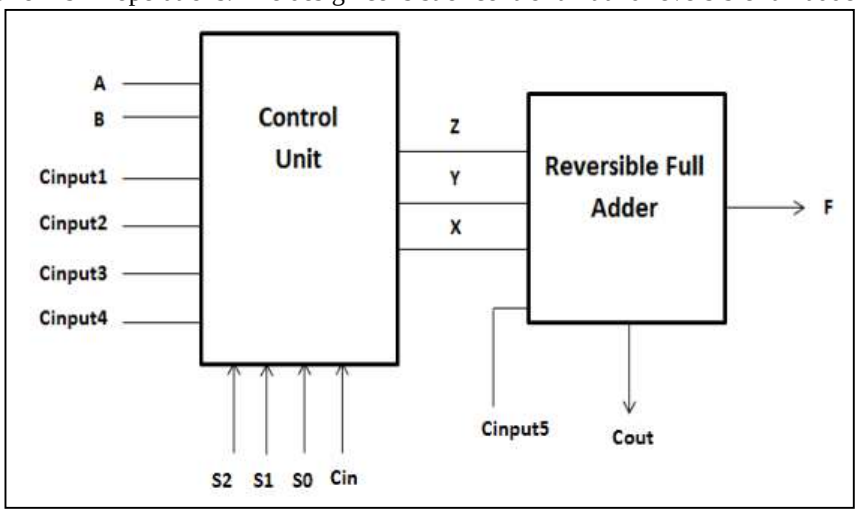


Fig. 2: Block diagram of First block of ALU

The proposed control unit and reversible full adder consist of 5 constant signals Cinput1,Cinput2,Cinput3,Cinput4,Cinput5, and 4 control signals s2 s1 s0 and Cin. The proposed control unit is designed using feynman, fredkin, and peres gates as shown in figure3.

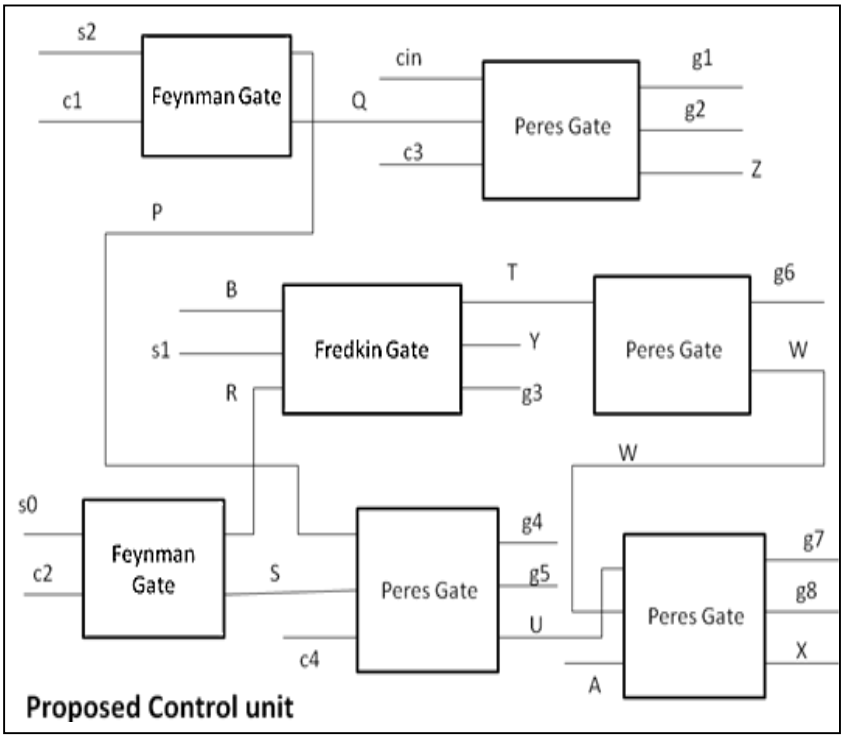


Figure3: Proposed block diagram of control unit

A. Multiplier:

In the proposed multiplier partial product generation is done by using toffoli gate (TG) as shown in figure5. The multi-operand addition is done by using the peres gate (PG) and HNG gates as shown in figure6. Peres gate can act as half adder by making the third input C=0. As it has one XOR and a AND operations in it . HNG can act as full adder by making the fourth input as D=0.

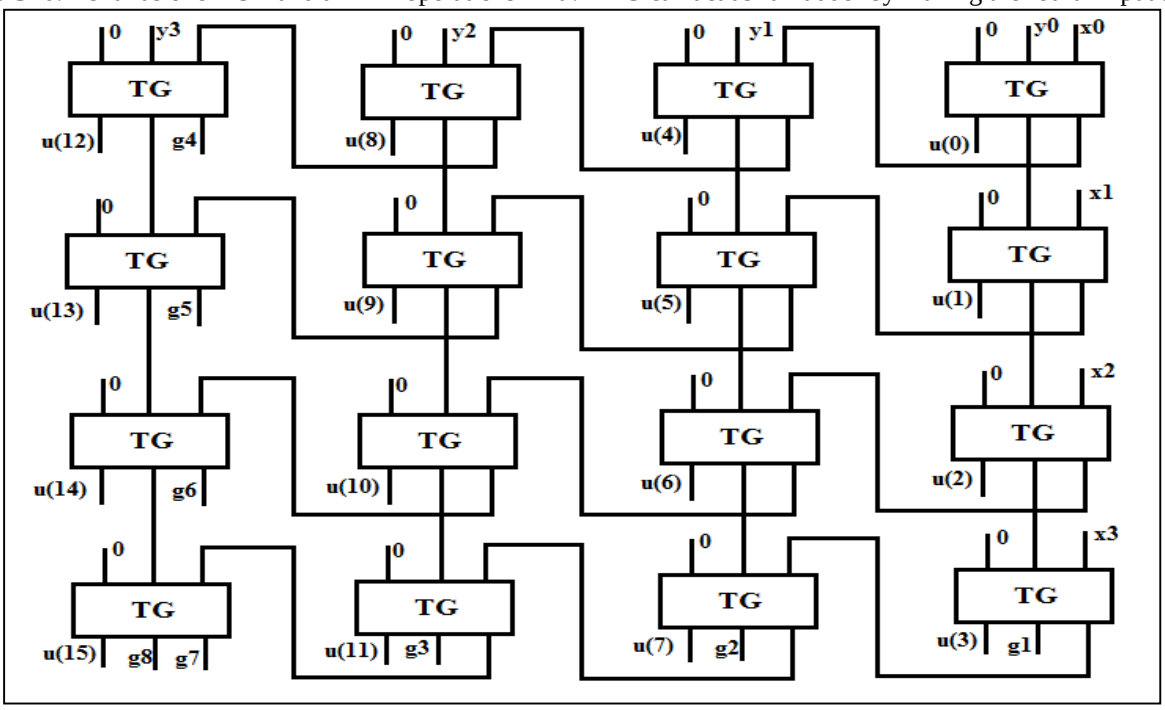


Fig. 5: Proposed block diagram of Partial Product Generation

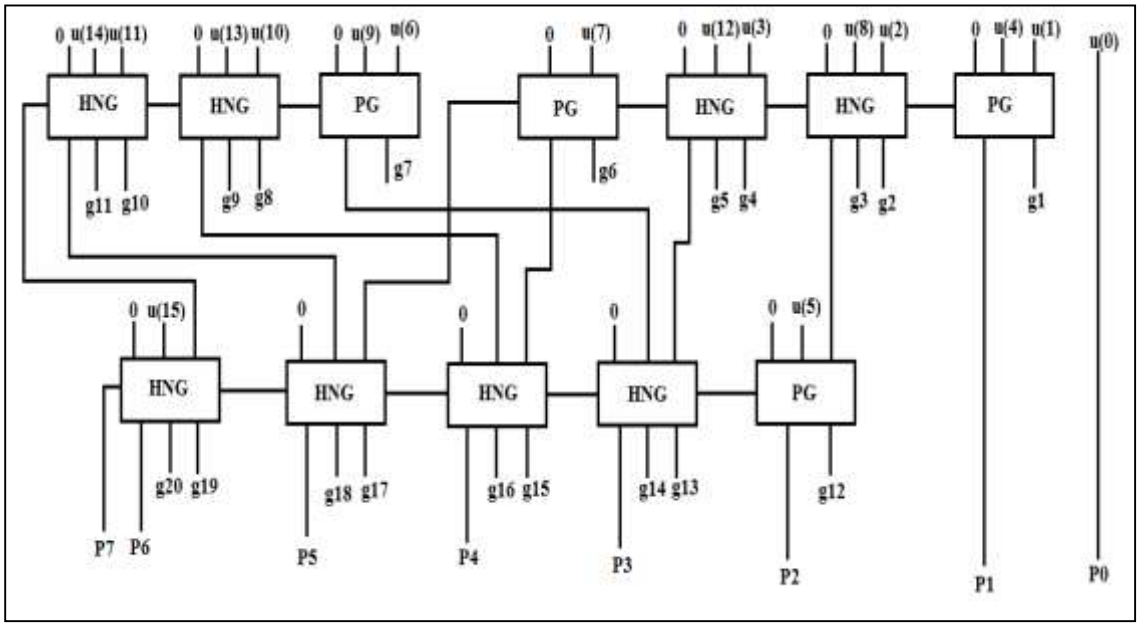
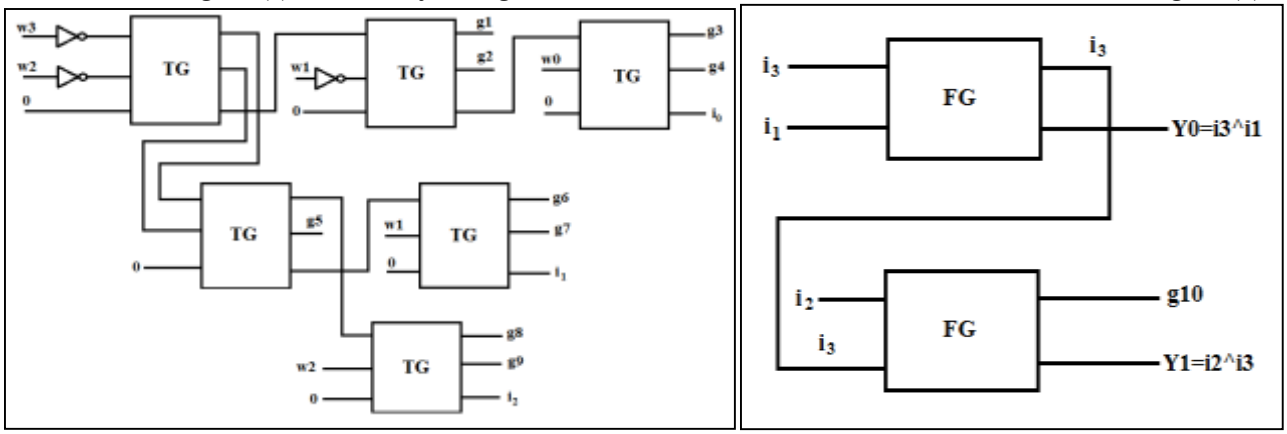


Fig. 6: Proposed block diagram of Multi-Operand Addition

B. Priority Encoder:

The proposed reversible 4:2 Priority encoder is designed by using 4 Toffoli gates (TG) from which i0,i1,i2, and i3 values are obtained as shown in figure7(a) and also Feynman gate is used to obtained the values of Y0 and Y1 as shown in figure7(b).



(a) (b)

Fig. 7: Proposed block diagram of reversible Priority encoder

C. Shifter:

The proposed reversible shift register is designed by using Peres gate and Feynman gate, which performs the arithmetic right shift operations as shown in figure8.

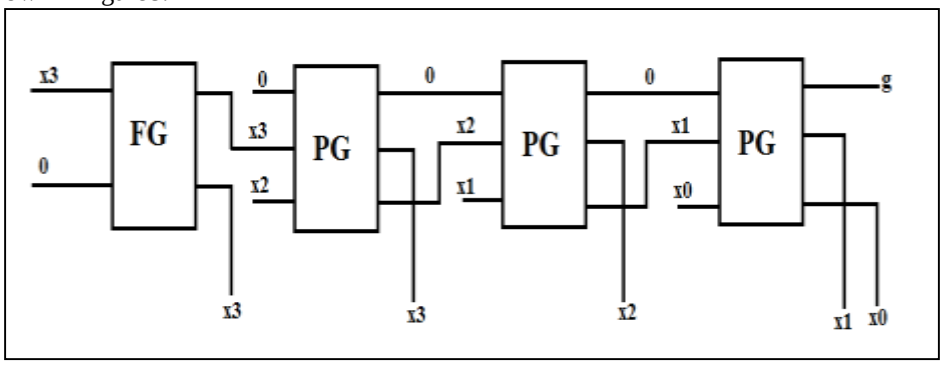


Fig. 8: Proposed block diagram of Shift register

D. Application of Proposed Reversible ALU for MAC Design:

The proposed ALU is very useful for MAC and CPU whose performance is dependent upon the efficiency of the ALU. In this section multiplier multiplies the two n-bit numbers and gives the 2n-bit result to adder, which adds the multiplier result to the previously accumulated result.

IV. RESULT AND DISCUSSION

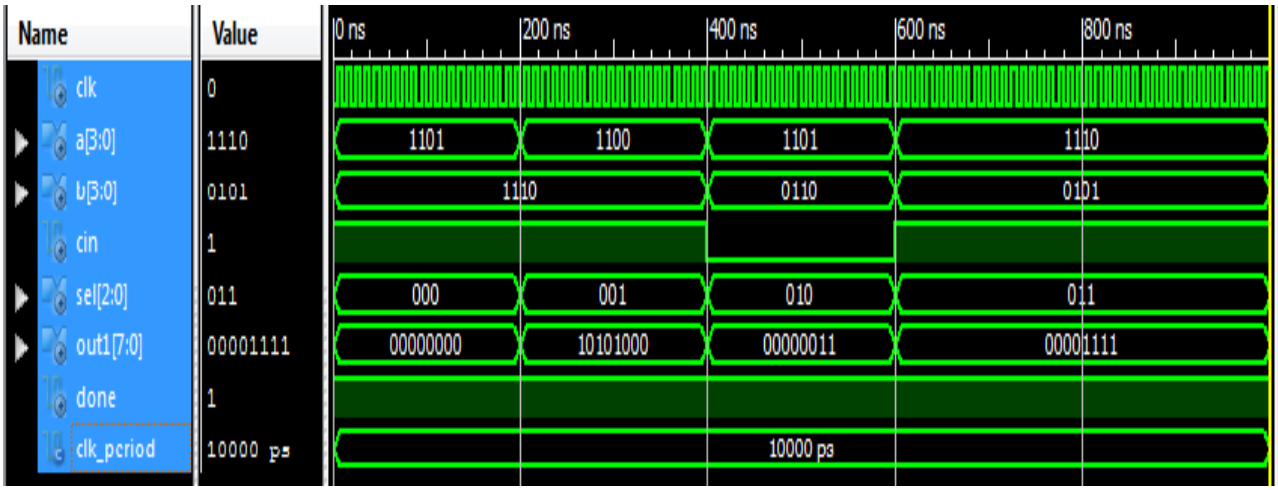


Fig. 9: Simulation results of proposed reversible ALU

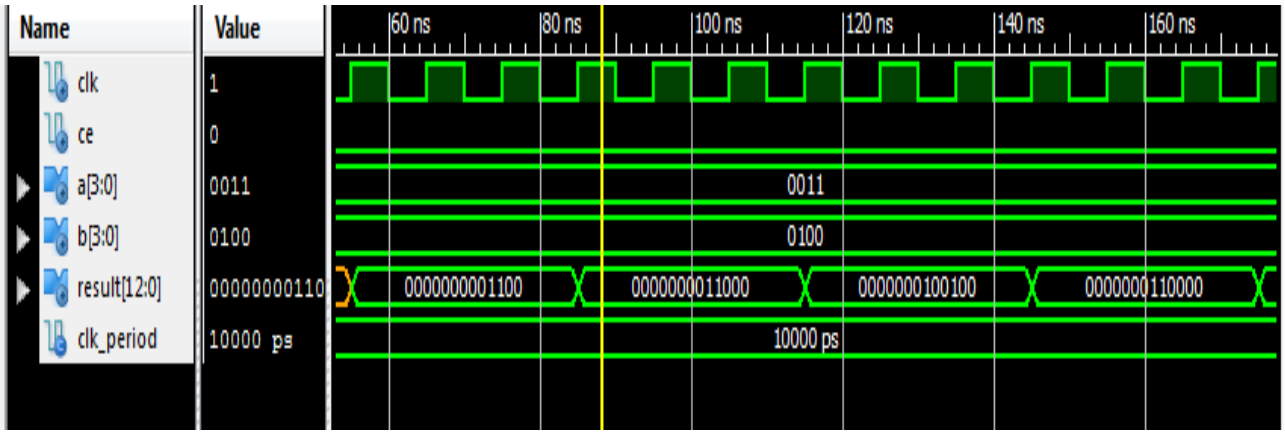


Fig. 10: Simulation results of MAC unit

V. CONCLUSION

The proposed reversible ALU offers the low power dissipation due to the use of reversible logic gates by reducing the quantum cost, garbage output, constant inputs and number of gates used to design the circuit. The proposed control unit plus reversible full adder is designed with less delay compared to existing [1]. The proposed multiplier circuit is designed with less garbage output compared to existing [7]. The proposed priority encoder design is a novel design.

ACKNOWLEDGEMENT

I thank, the management, Principle, HOD and staff of VLSI and ES Department, Visvesvaraya Technological University (VTU), Belagavi, Karnataka, India and my special thanks to my guide Dr. Meghana Kulkarni, Associate professor, Dept of VLSI and ES for encouraging me for this work.

REFERENCES

[1] Lenin Gopal, Nor Syahira Mohd Mahayadin, Adib Kabir Chowdhury, Alpha Agape Gopalai, and Ashutosh Kumar Singh, "Design and Synthesis of Reversible Arithmetic and Logic Unit (ALU)", International Conference on Computer, Communication, and Control Technology (I4CT 2014), September 24, 2014.

[2] Pankaj Kumar Israni, "Design and Synthesis of Low Cost Reversible Arithmetic and Logic Unit (ALU)", International Journal of Advanced Research in Computer Science and Software Engineering Volume 5, Issue 3, March 2015.

[3] Kamaraj Arunachalam, Marichamy Perumalsamy, C. Kalyana Sundaram, and J. Senthil Kumar, "Design and Implementation of a Reversible Logic based 8-Bit Arithmetic and Logic Unit", International Journal of Computers and Applications, Vol. 36, No. 2, 2014.
[4] Darshan H, Mohanraj R, Kavya H B, Monisha U K, and Saroja Maralabhavi, "Design and Synthesis of 8 Bit Reversible Arithmetic & Logical Unit (ALU)", ITSI Transactions on Electrical and Electronics Engineering (ITSI-TEEE), Volume -3, Issue -3, 2015.
[5] Naman Sharma, Rajat Sachdeva, "Power Efficient Arithmetic Logic Unit Design using Reversible Logic", International Journal of Computer Applications (0975 – 8887) Volume 128 – No.6, October 2015.
[6] Maneet, Naveen Sharma1 and Virender Singh, "16 bit ALU Design using Reversible Logic", International Journal of Electrical and Electronic Engineering and Telecommunication, Vol. 3, No. 4, October 2014.
[7] Aakash Babu Suresh, "Design and Optimization of Reversible Multiplier Circuit", International Journal of Computer Applications (0975 – 8887) Volume 52– No.10, August 2012.