Power System Stability Analysis on System Connected to Wind Power Generation with Solid State Fault Current Limiter

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Abstract

The main aim of this paper is to model a Solid State Fault Current Limiter (SSFCL) and test the SSFCL on a test system. The test system consists of a GRID and WTPG. Distributed generations (DGs) are predicted to perform an increasing role in the future electrical power system. Expose of the DG, can change the fault current during a grid disturbance and disturb the existing distribution system protection. Fault current limiters (FCLs) can be sorted into L-types (inductive) and R-types (resistive) by the fault current limiting impedance. In this paper, a new SSFCL has been proposed. SSFCLs can provide the fast system protection during a rigorous fault. The act of dynamic damping enhancement via the SSFCL is appraised in the presence of the wind-turbine power generation. Hence, its efficiency as a protective device for the wind-turbine system is confirmed via some case studies by simulation based on the MATLAB/SIMULINK
Keywords: Distributed Generation (DG), Fault, Grid, Insulated Gate Bipolar Transistor (IGBT), Solid-state fault current limiter (SSFCL), Wind-turbine power generation (WTPG)

I. INTRODUCTION

When electric power systems are expanded and become more interconnected, the fault current levels increase beyond the capabilities of the existing equipment, leaving circuit breakers and other substation components in over-duty conditions. Fault current arises due to line to line fault or line to ground fault (symmetrical or asymmetrical fault) in the power system. This fault results in sudden increase of current for small interval of time. Circuit breakers, sometimes, cannot handle the intense level of faults, so they fail to break the peak rest of fault current and is enough to burn the insulation and conductor. Handling these increasing fault currents often requires the costly replacement of substation equipment or the imposition of changes in the configuration by splitting power system that may lead to decreased operational flexibility and lower reliability.

To protect the electrical equipment the fault current should be reduced and normalized. The circuit breaker was before used to isolate the fault Section. If the fault current is more than interruption capacity of circuit breaker, it easily damages the electrical equipment in the circuit. An alternative is to use Fault Current Limiters (FCL) to reduce the fault current to a low acceptable level. So that the existing switchgear still be used to protect the power grid. So a new technology is adopted to reduce the fault current and to enhance the security of power system. This is the novel technique for reducing high fault current using high temperature super conducting fault current limiter (FCL).Now days the generation system has become more complex and more generation load is interconnected and control of fault current is done by splitting the power system into zones.

There are many types of FCLs like current limiting fuses, superconducting FCL, resonance LC FCL. Some of these create problems such loss of power system stability, high cost and increase power losses and ultimately leads to decreased operational flexibility and lower reliability. The basic operation of resonant LC FCL is that the impedance of a LC-resonant circuit can be tuned so that the impedance of the device during steady state operation is approximately zero. During a fault, power electronic switches isolate a capacitor or inductor from the device, introducing large impedance into the system. The limitations of resonance based limiters are that they can make voltage sags during faults, current limitation efficiency declines as distance from substation increases, large infrastructure for capacitors is required, and tuning of these devices is essential to guarantee low impedance. The high cooling requirements of superconducting FCL is the requirement of complex, bulk and costly cooling equipment. In order to eliminate these difficulties Solid State Fault Current Limiters (SSFCL) are used.

II. CONCEPT OF PROPOSED SSFCL AND TEST SYSTEM

A. Proposed SSFCL Model:

The schematic diagram of proposed Solid State Fault Current Limiter in parallel to a resistor is shown in figure.1. SSFCL consists of four diodes D1, D2, D3, D4 connected in such a way that diode D1 and D2 conduct for positive half cycle and diode D3 and D4 conduct for negative half cycle. An IGBT in placed in between the diodes which is used as a switch for operating the fault current limiter.

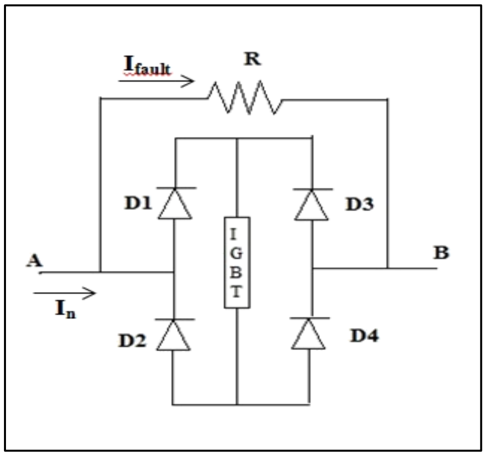

Fig. 1: Proposed SSFCL with a Resistor Connected In Parallel

In this SSFCL, when a fault occurs then there is a drop in voltage which is measured by the calculated the RMS value of the voltage. If the voltage drop is below certain value then the IGBT switch is turned off. Thus the fault current flows through the resistor and gets dissipated. Thus the current comes to normal value within few milliseconds.

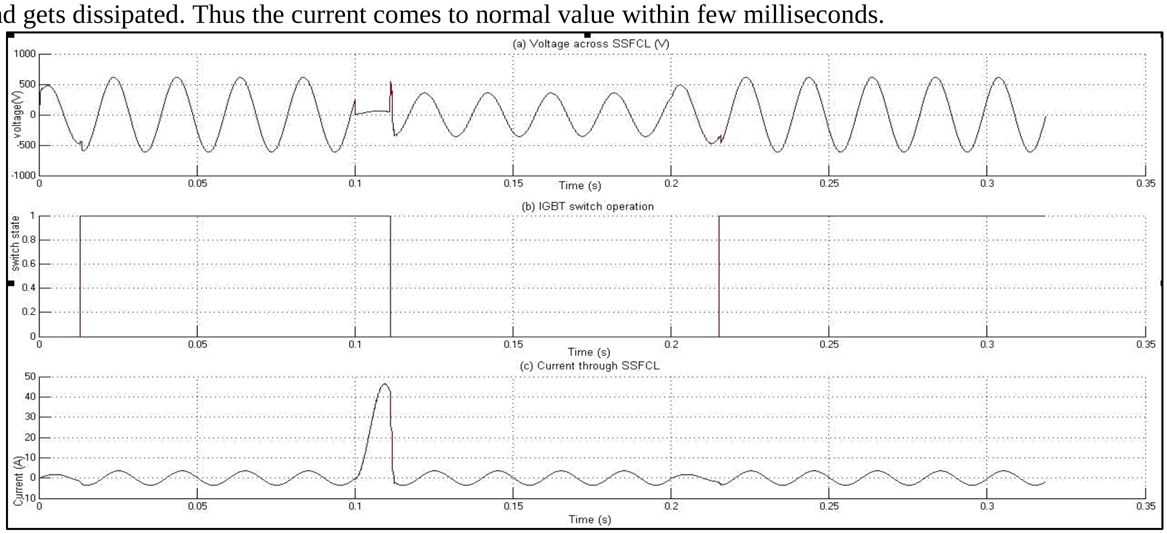

Fig. 2: (A) Voltage across SSFCL, (B) IGBT Switch Operation, (C) Current through SSFCL

The operation of the SSFCL is shown in the figure 2. The fault occurs at 0.1 seconds. It is seen that during fault the voltage decreases from 614V to 357V and the current rises to 10 times of the normal current. The IGBT turns off at 0.1113 seconds and the fault current passes through the resistor and the value of current reduces to normal value and voltage decreases to a value based upon the resistance.

B. Test System:

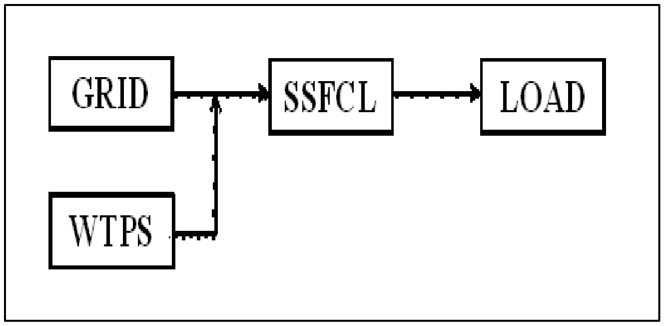

Fig. 3: Test system for SSFCL

The grid consist a voltage source with 440 phase-phase voltage and 50 Hz. The Wind Turbine Power System (WTPS) consists of a turbine with 1.5MW generation at constant wind speed of 13 m/s. The wind turbine is connected to a 50KW load. The extra generated power is connected to grid which is connected to load of 10MW.

III. IMPACT OF SSFCL ON SYSTEM

The simulation of normal system without SSFCL is simulated in MATLAB/SIMULINK software as shown in the figure 4. A three phase symmetrical fault occurs at 0.1 second and clears at 0.2 second.

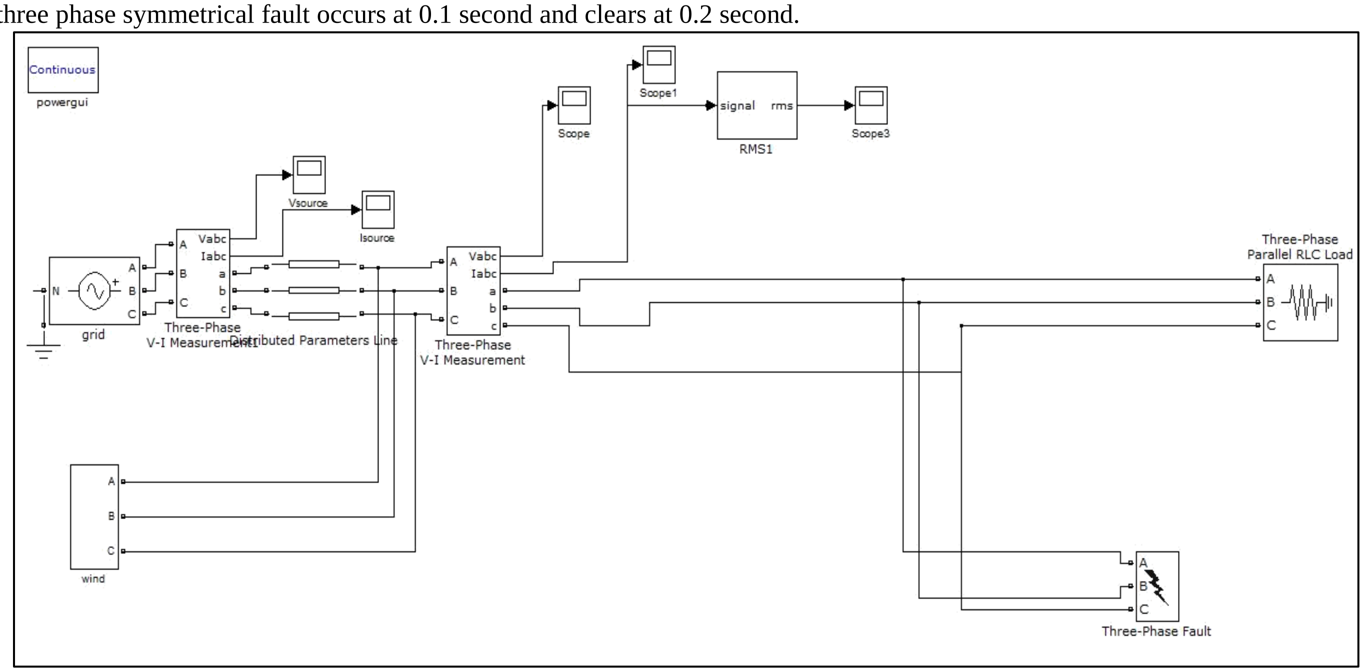

Fig. 4: The MATLAB/SIMULINK Simulation Model without SSFCL.

The simulation of the proposed SSFCL system is simulated in MATLAB/SIMULINK software as shown in the figure 5. The SSFCL is connected near the load and 3 phase symmetrical fault is simulated.

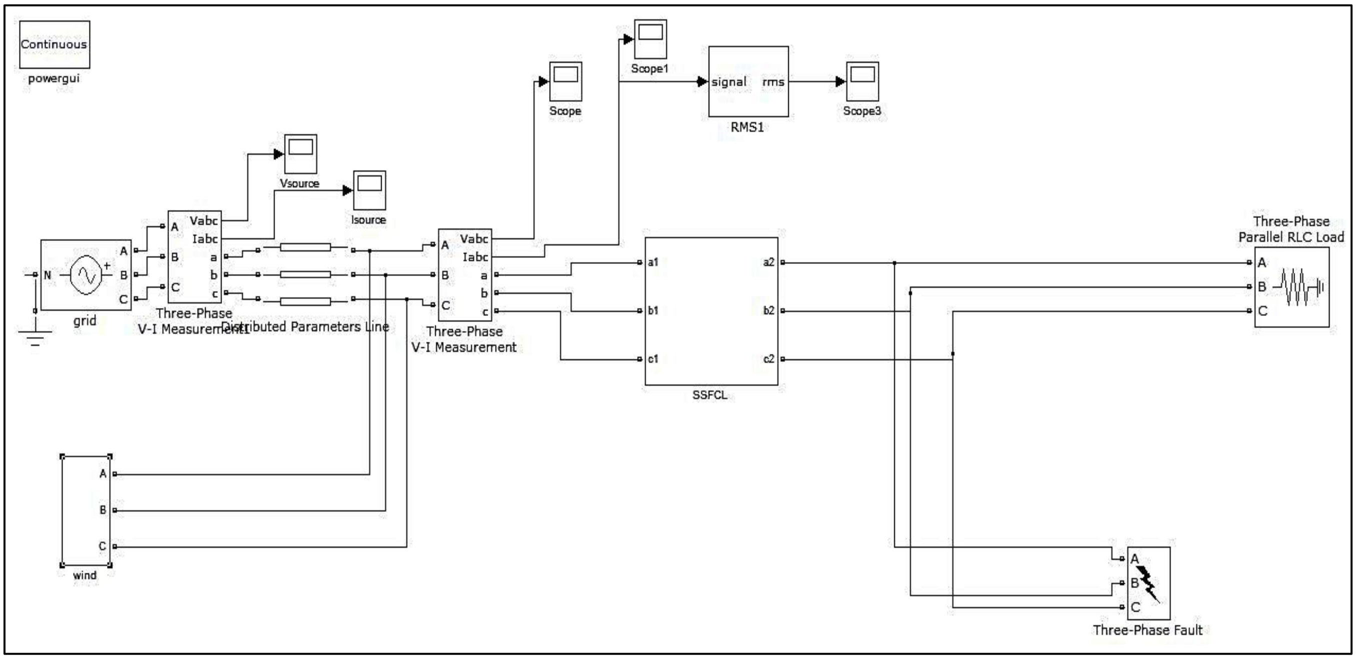

Fig. 5: The MATLAB/SIMULINK simulation model with SSFCL

IV. SIMULATION RESULTS

The simulation of normal system without SSFCL, shown in figure 4, for symmetrical three phase fault is simulated and the system voltage and current is measured as shown below.

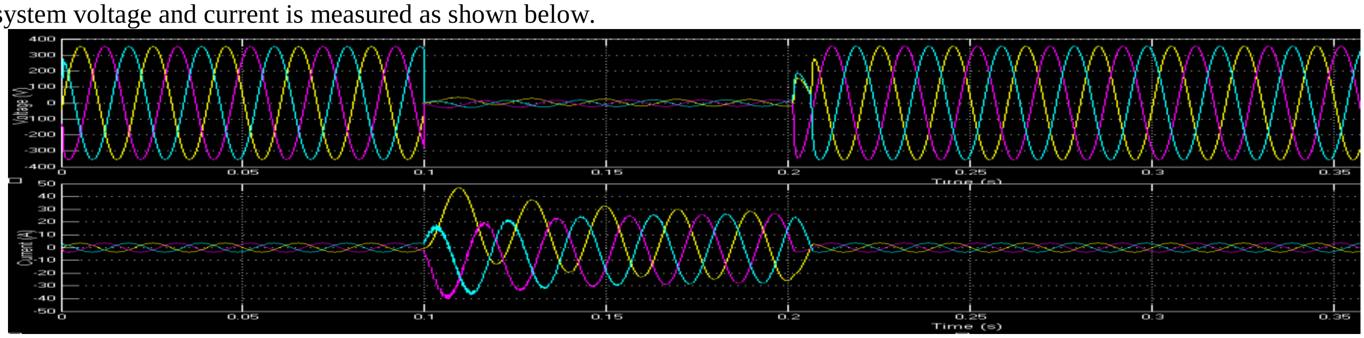

Fig. 6: Vsystem And Isystem Of System Without SSFCL For Symmetrical Three Phase Fault

From the above plot it is seen that during normal operation the system voltage was 355V and current was 3.5A. When a three phase symmetrical fault is applied at 0.1 second then the current rises to 47A and the voltage decreases to 35.7V. The fault current decreases slowly which diminished after the fault is cleared. Thus if a SSFCL is applied then the current is decreased within milliseconds as shown below. The proposed SSFCL model is tested on the test system and the results are plotted. The system model is shown in figure 5.

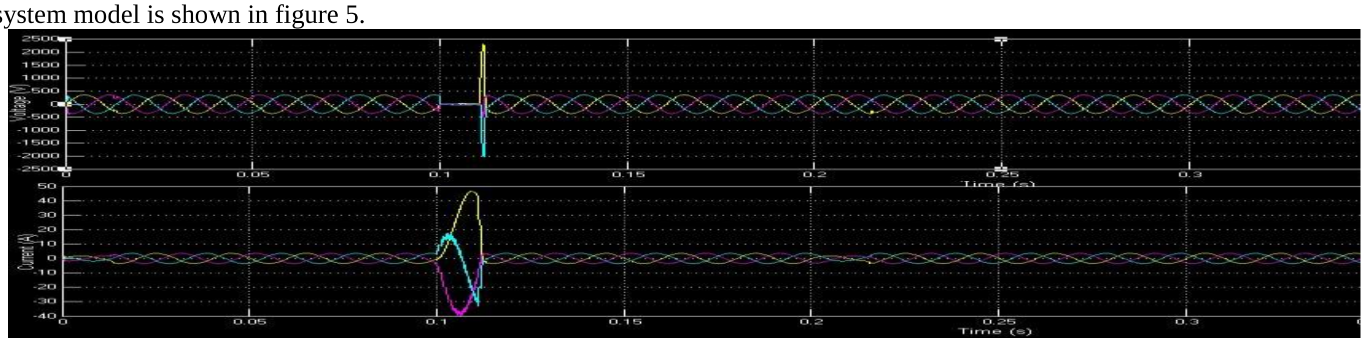

Fig. 7: Vsystem And Isystem Of System With SSFCL For Symmetrical Three Phase Fault

From the above plot it is seen that during normal operation the system voltage was 355V and current was 3.5A. When a three phase symmetrical fault is applied at 0.1 second then the current rises to 47A and the voltage decreases to 35.7V. Due to the

SSFCL the current decreases to normal within 0.111 second. From the plot it is seen that when the current suddenly reduces to normal there is a voltage spike which can be mitigated by using a surge arrester across the resistor.

The effect of the location of SSFCL and location of fault are tested and the results are plotted as different cases as shown Below.

1) Case 1 – The ssfcl is placed near the load and the fault occurs in between ssfcl and load
2) Case 2 – The ssfcl is placed near the load and the fault occurs before the ssfcl
3) Case 3 – The ssfcl is placed near the dg and the fault occurs in between the ssfcl and the grid
4) Case 4 – The ssfcl is placed near the dg and the fault occurs in between the ssfcl and the dg
5) Case 5 – The ssfcl is placed near the dg and the fault occurs near the load
6) Case 6 – The ssfcl is placed near the load and the fault occurs near the dg

Table – 1

Case no.	*Location of SSFCL*	*Location of Fault*	*Effect*
Case 1	*Near load*	*Near load after SSFCL*	*The fault current increases nearly 10 times but after 0.111s it decreases to normal condition.*
Case 2	*Near load*	*Near load before SSFCL*	*Even if the FCL operates the fault current doesn't reduce because the fault current doesn't passes through the FCL circuit.*
Case 3	*Near DG*	*Between SSFCL and grid*	*FCL decreases the current from the DG but not from the grid.*
Case 4	*Near DG*	*Between SSFCL and DG*	*Similar to case 3 but FCL decreases current from grid . Fault current is supplied from DG.*
Case 5	*Near DG*	*Near load*	*Similar to case 3.*
Case 6	*Near load*	*Near DG*	*Similar to case 2.*

V. CONCLUSION

In this paper, a Solid State Fault Current Limiter (SSFCL) is modeled and tested with a system with a programmable voltage source interconnected with Wind Turbine Power System and load. The results obtained show that whenever a fault (like L-G, L-L-G, three phase fault) occurs, without the fault current limiter the current will rise to about 10 times of the normal value. If SSFCL is used then the value of current is reduced to normal value within 1ms. Thus it is beneficial to place a SSFCL in the circuit. The location of the SSFCL and the Fault also effects the operation. The location of the SSFCL must be in the path of the fault current from the source to fault else the protection will not be provided by the SSFCL as shown in table 1.

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