Modeling of Diode Clamped Multilevel Inverter using Sinusoidal PWM

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Abstract

Multilevel inverter is an important alternative technique in high power, medium voltage power control. Multilevel inverter topology is classified in to diode clamped multilevel inverter (DCMLI), flying capacitors multilevel inverter, cascaded inverter with separate dc source. This project presents diode clamped multilevel inverter with sinusoidal pulse width modulation (SPWM) framework. The carrier based SPWM technique is developed to facilitate its implementation in diode clamped multilevel inverter. Diode clamped multilevel inverter using MOSFET as switching device is used in this particular project.
Furthermore, in this study reduction of harmonics has been stressed on using diode clamped multilevel inverters. It also states the adverse effects of Total Harmonic Distortion (THD) on generation and transmission equipments. It also explains about Common Mode Voltage and its effects in brief. Multilevel Inverters have been designed, modeled and simulated and the output results have been depicted in the form of waveforms, THD analysis modules using MATLAB SIMULINK and the results are systematically tabulated.

Keywords: Adjustable Speed Drives, Multilevel Inverters, PWM, THD, DCMI

I. INTRODUCTION

One of the major effects of power system harmonics is to boost the current in the power system. This is predominantly in one of the case for the third harmonic, this cause quick increase in the zero sequence current and as a result increases the current in the neutral conductor. This effect requires special concern in the design of an electric power system to serve non-linear loads. In adding up to the increased line current, different parts of electrical equipment can suffer from harmonics on the power system.

Harmonic voltages and currents in an electric power system are due to the result of non-linear electric loads. In power grid harmonic frequencies are a frequent cause of power quality problems. Harmonics in power system result in high increase of heating in the equipment and conductors, torque pulsations in motors, and misfiring in variable speed drives etc.

Current harmonics are cause due to non-linear loads. When the non-linear load such as a rectifier is coupled to the power system it draws a current which is not compulsory to be sinusoidal. The current waveform might become somewhat complex, depending on the nature of load and its interface with other components of the power system. Despite of how complex the current waveform become, it can be described through Fourier series analysis, this is possible to decompose it into a sequence of simple sinusoids, Starting at the fundamental frequency and occur as integer multiples of the fundamental frequency.

Voltage harmonics are mainly caused due to current harmonics. The voltage provided by voltage source is distorted by the harmonic current this is due to source impedance. If the supply impedance of voltage is small, current harmonics cause only small voltage harmonics.

A. Total Harmonic Distortion

Total harmonic distortion, or THD is a common measurement of the level of harmonic distortion present in power systems. THD is defined as the ratio of total harmonics to the value at fundamental frequency.

$$\mathrm{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}}{V_1}$$

where V_n is the RMS voltage of *n*th harmonic and $n = 1$ is the fundamental frequency.[1]

II. MULTILEVEL INVERTER

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The unique structure of multi- level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as motor steps are included in the waveform the harmonic distortion of the output wave decrease, approaching zero as the number of levels approaches infinity.

Hence Multi-level inverters offer a better choice at the high power end because the high volt- ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones.

The basic three types of multilevel topologies used are:

- Diode clamped multilevel inverters
- Flying capacitors multilevel inverter or Capacitor clamped multilevel inverter
- Cascaded inverter with separate dc source.

A. Diode-Clamped Multilevel Inverter:

The diode-clamped type inverter is used for experimentations in this project. Such inverter employs the technique of proportional stepping harmonic elimination type to control switching equipment in the circuit for providing appropriated waveform and increasing the efficiency at high loading. The diode-clamp and modulate principle are implemented to control the output waveform approaching to the sine-wave as close as possible.

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is *Vdc*. An *m* level inverter needs (*m*-1) voltage sources, 2(*m*-1) switching devices and 2 (*m*-2) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform.

III. MODELLING OF INVERTERS

A. Two Level Inverter:

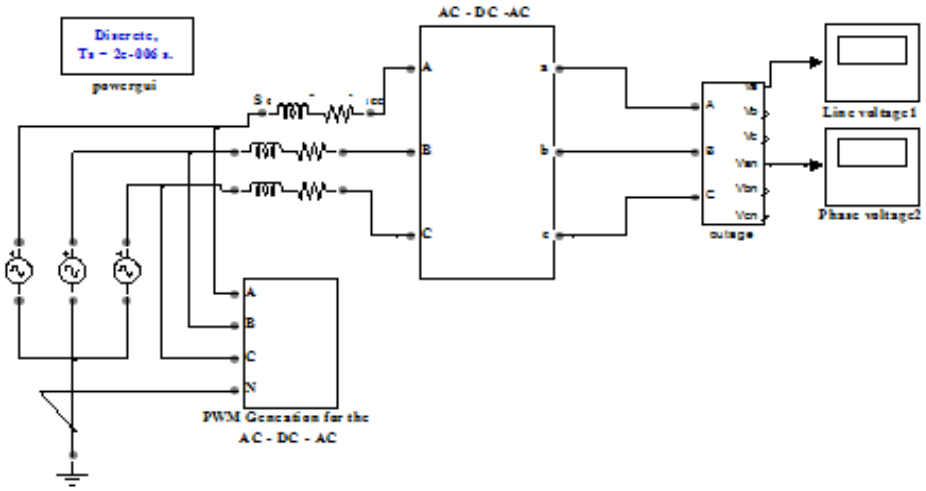


Fig. 1: Two level inverter simulink model

1) PWM Signal Generation

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are two switch combinations to synthesize two-level voltages across a and n.

- Voltage level Van= Vdc/2, turn on the switch Sw1.
- Voltage level Van= 0, turn off the switches.
- Voltage level Van= - Vdc/2 turn on the switch Sw1′.

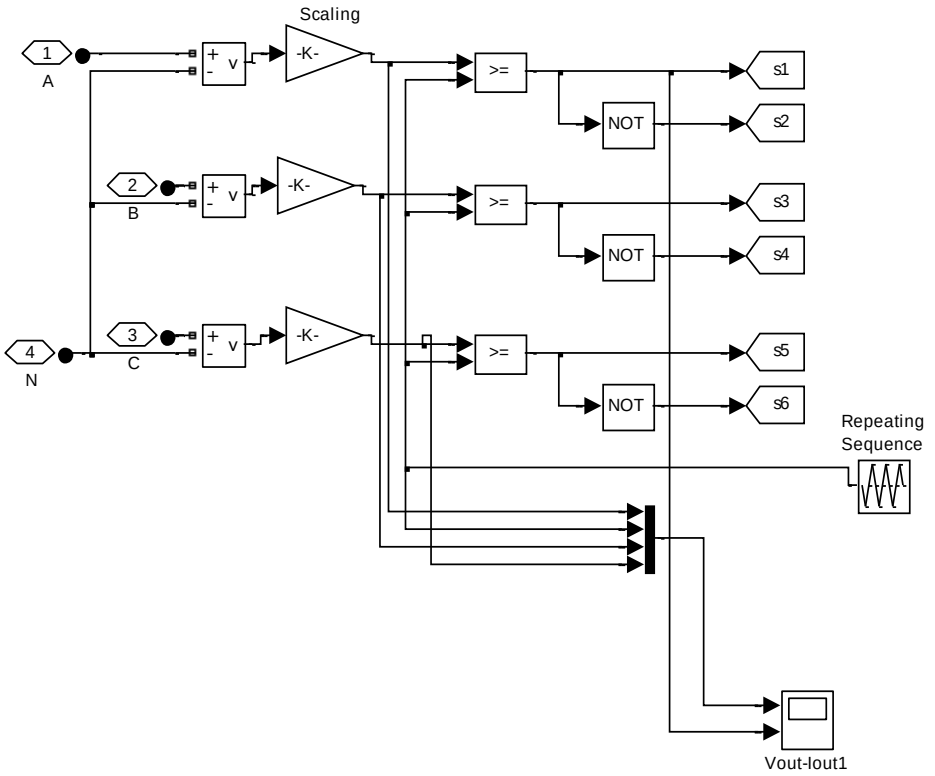
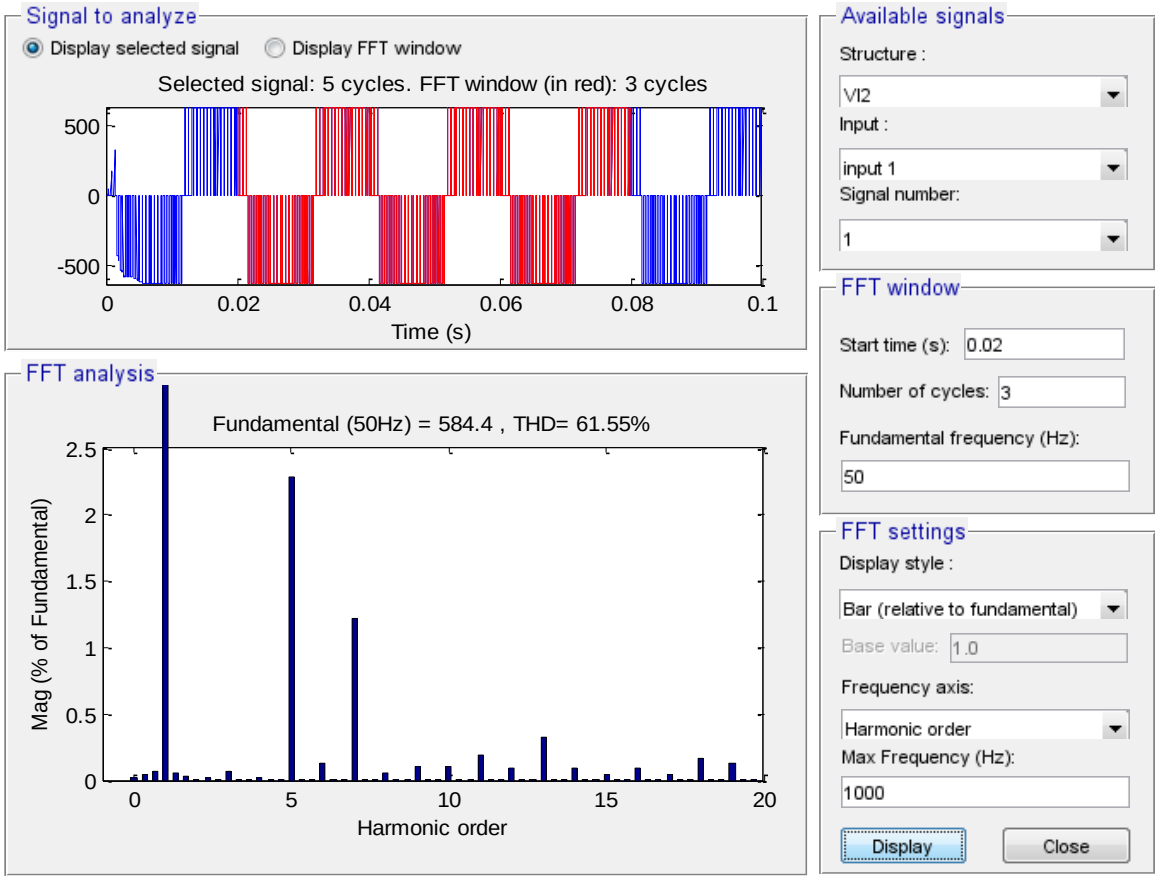


Fig 2: PWM signal generation

2) Line and Phase Voltage Thd Analysis:



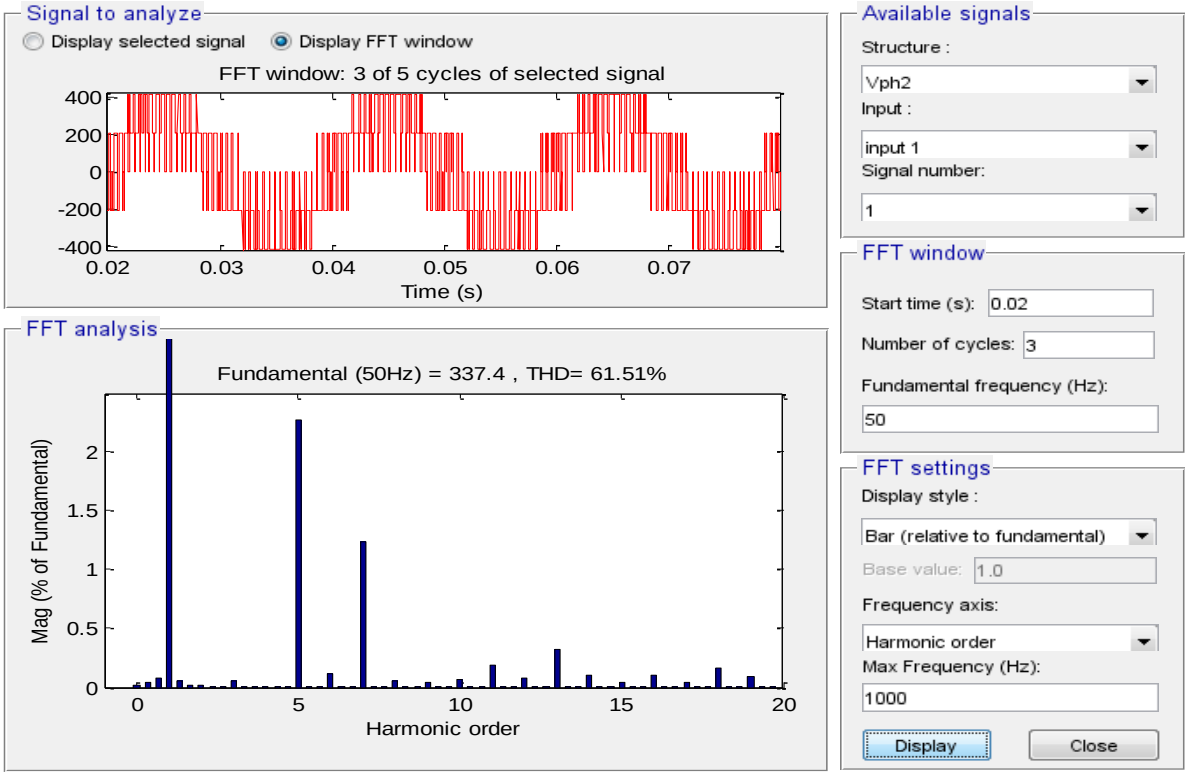


Fig. 3: Line And Phase Voltage THD Analysis

B. Three Level Inverter:

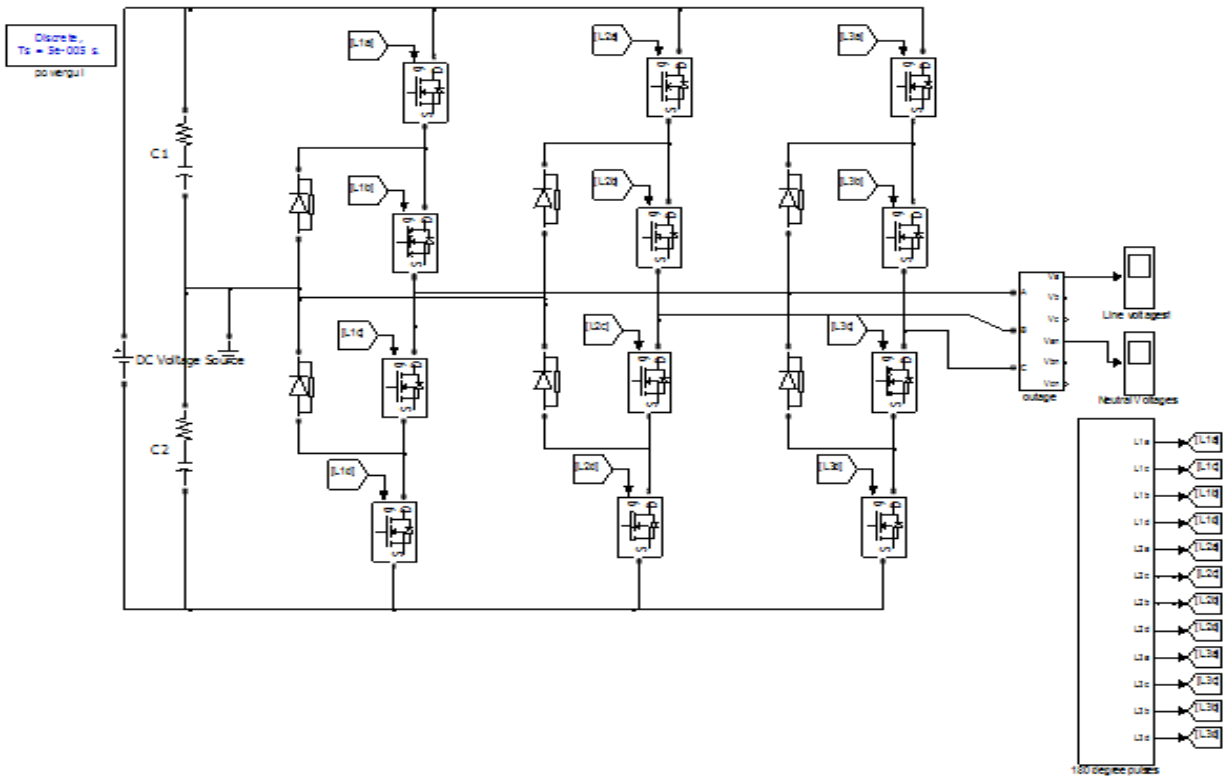


Fig. 4: Three level inverter simulink model

Figure shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2.

For dc bus voltage Vdc, the voltage across each capacitor is Vdc/2 and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

- Voltage level Van= Vdc/2, turn on the switches Sw1and Sw2.
- Voltage level Van= 0, turn on the switches Sw2 and Sw1′.
- Voltage level Van= - Vdc/2 turn on the switches Sw1′, Sw2′.

1) PWM Signal Generation:

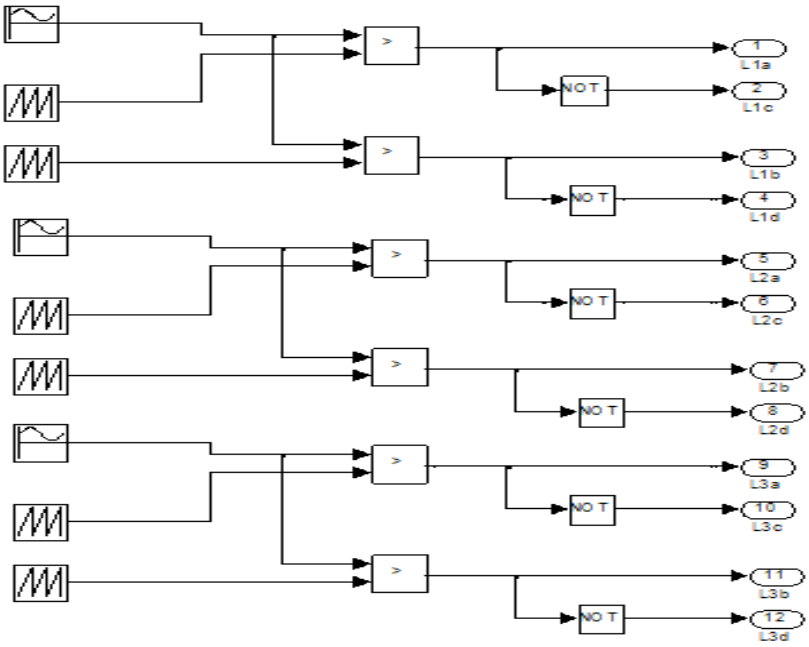
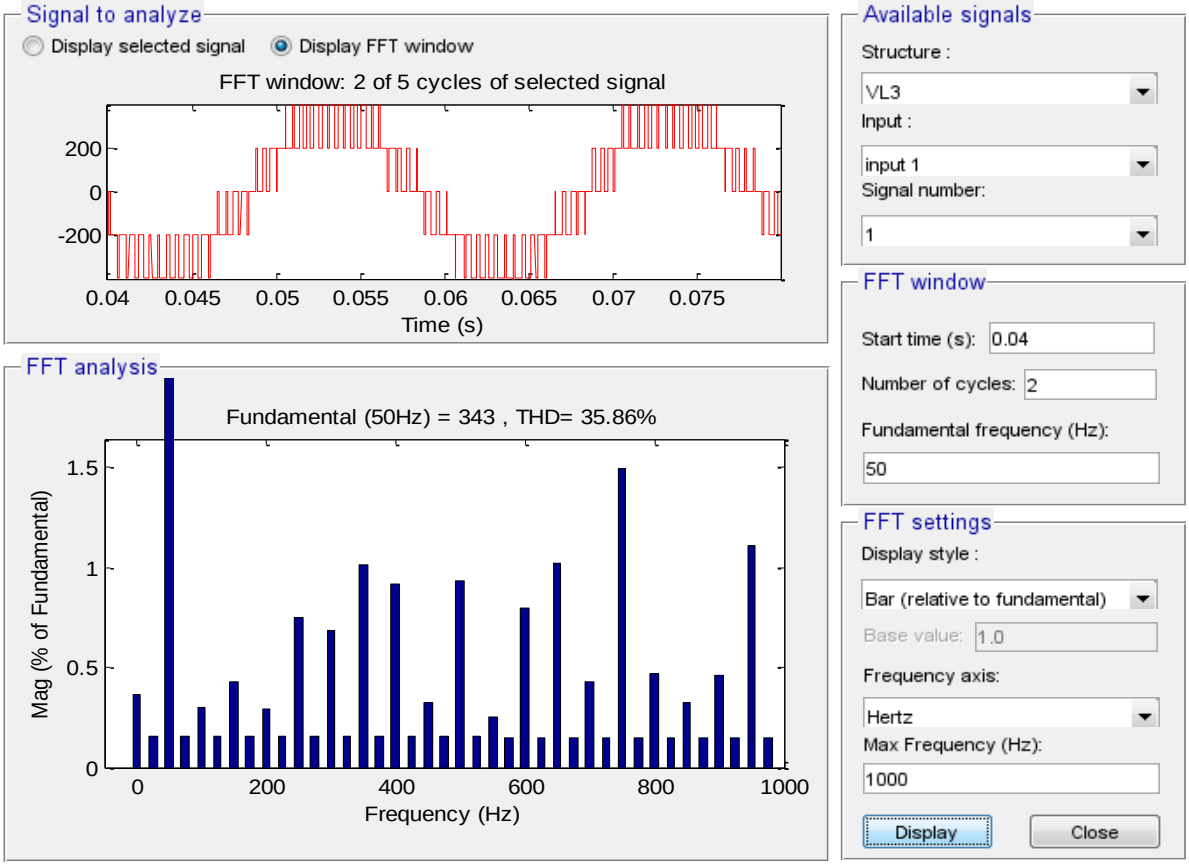


Fig. 5: PWM signal generation

2) Line And Phase Voltage THD Analysis:



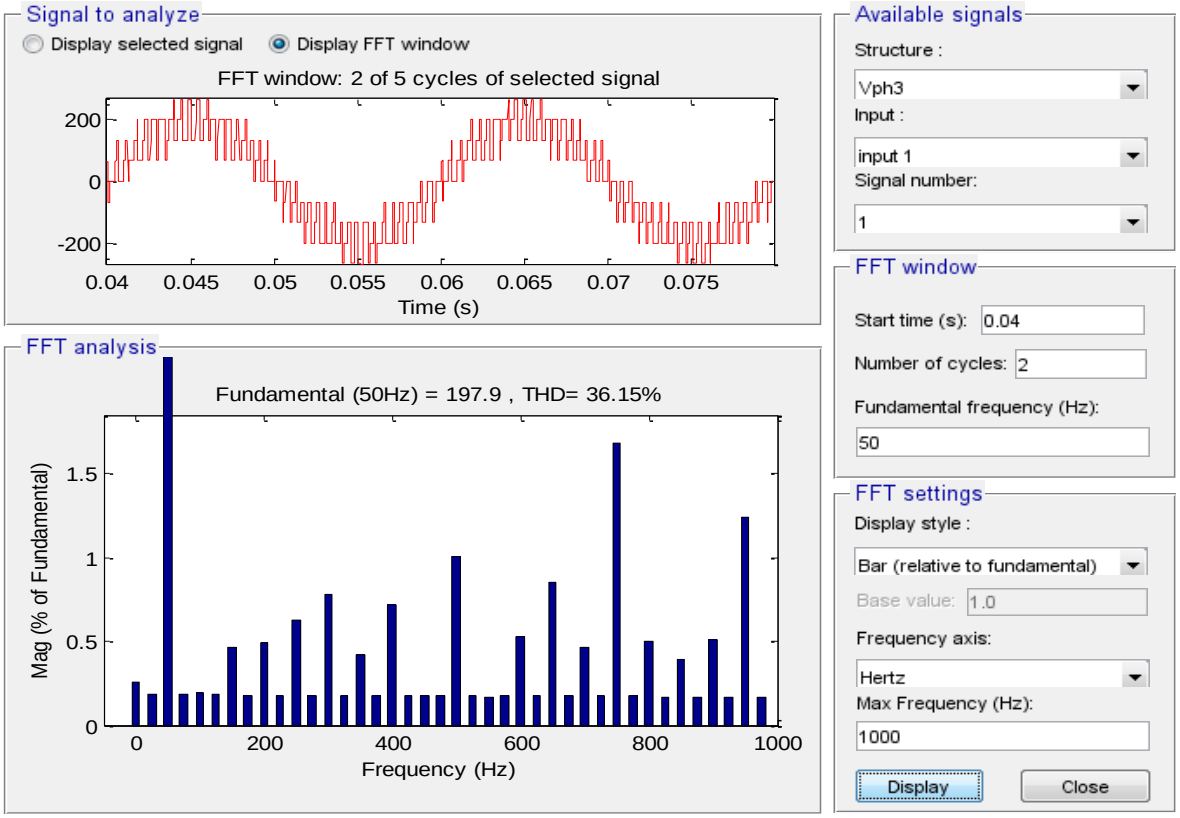


Fig. 6: Line and Phase Voltage THD analysis

C. Five Level Inverter:

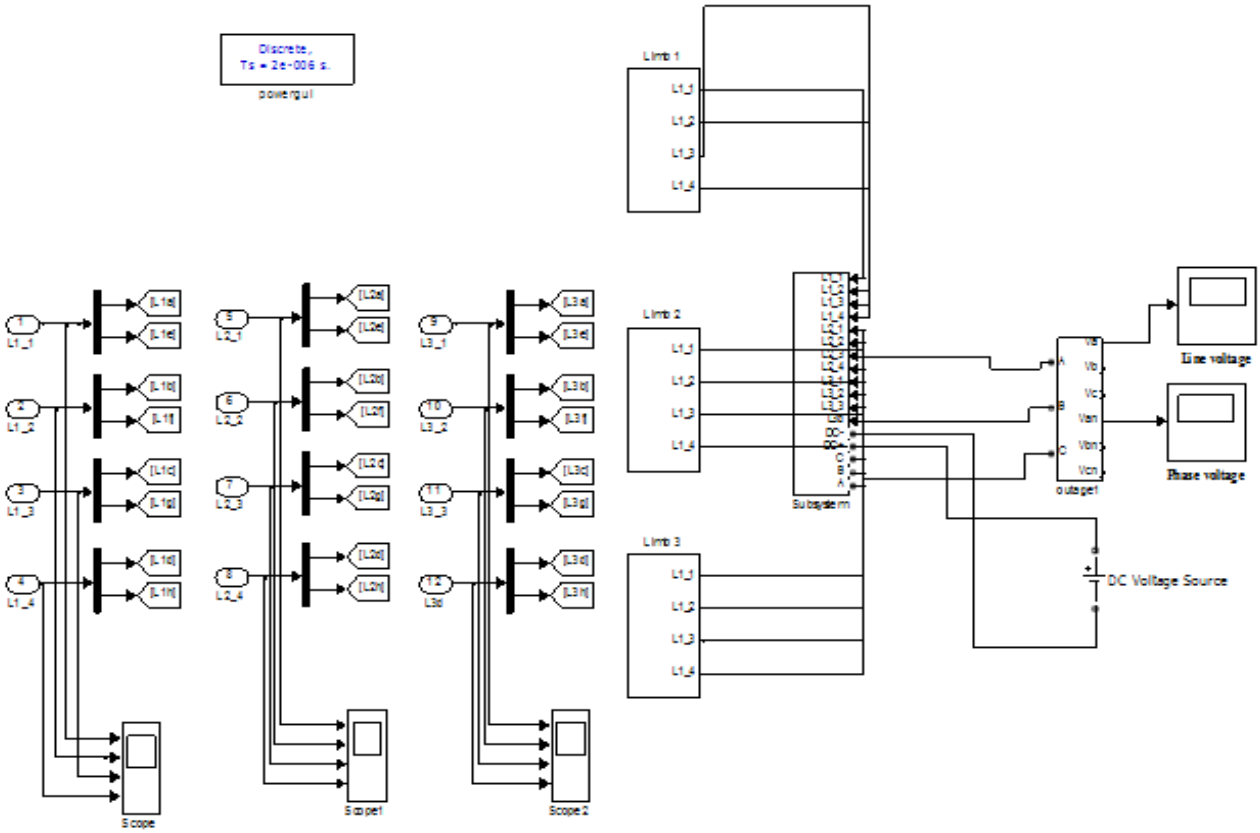


Fig 7: Five level simulation model

1) PWM Signal Generation:

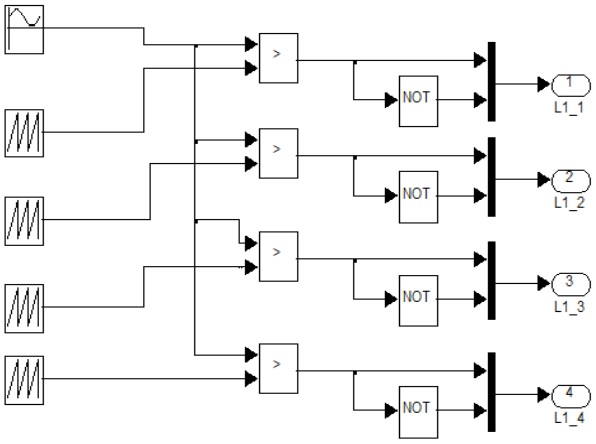


Fig. 9: PWM signal generation

2) Five Level Diode Clamped Circuit:

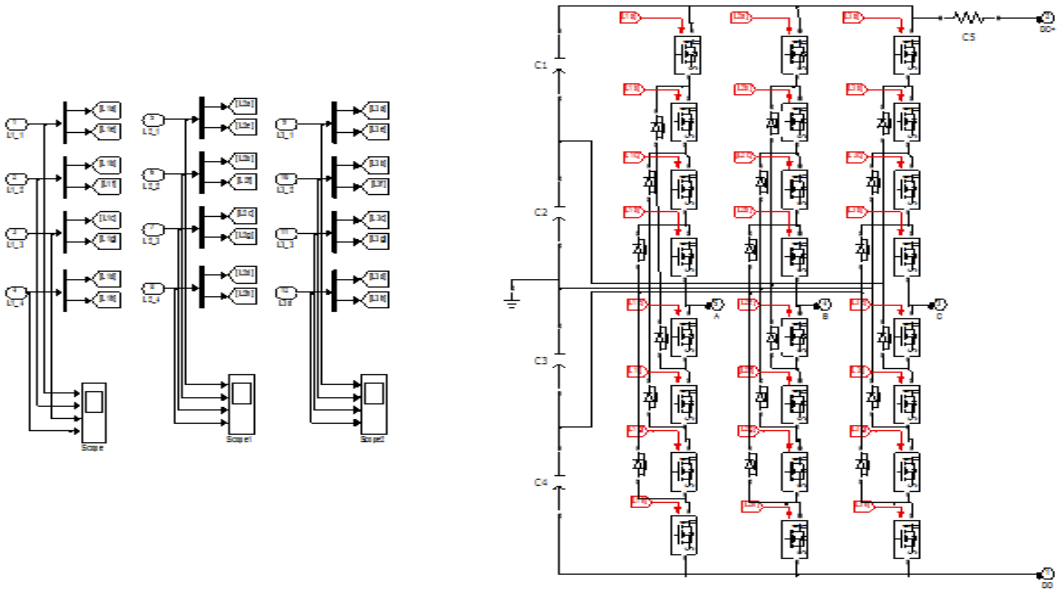


Fig. 8: Five level inverter simulink model

Figure shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes.

The order of numbering of the switches for phase a is Sw1, Sw2, Sw3, Sw4, Sw1', Sw2', Sw3' and Sw4'.

For example to have Vdc/2 in the output, switches Sw1 to Sw4 should conduct at the same time. For each voltage level four switches should conduct.

The steps to synthesis the five level phase a output voltage in this work are as follows:

- For phase a output voltage of Van=0, two upper switches Sw3, Sw4 and two lower switches Sw1' and Sw2'are turned on.
- For an output voltage of Van=Vdc/4, three upper switches Sw2, Sw3, Sw4 and one lower switch Sw1' are turned on.
- For an output voltage of Van=Vdc/2, all upper switches Sw1 through Sw4 are turned on.
- To obtain the output voltage of Van= -Vdc/4, upper switch Sw4 and three lower switches Sw1', Sw2' and Sw3'are turned on.
- For an output voltage of Van = -Vdc/2, all lower switches Sw1' through Sw4' are turned on.

3) Line And Phase Voltage Thd Analysis:

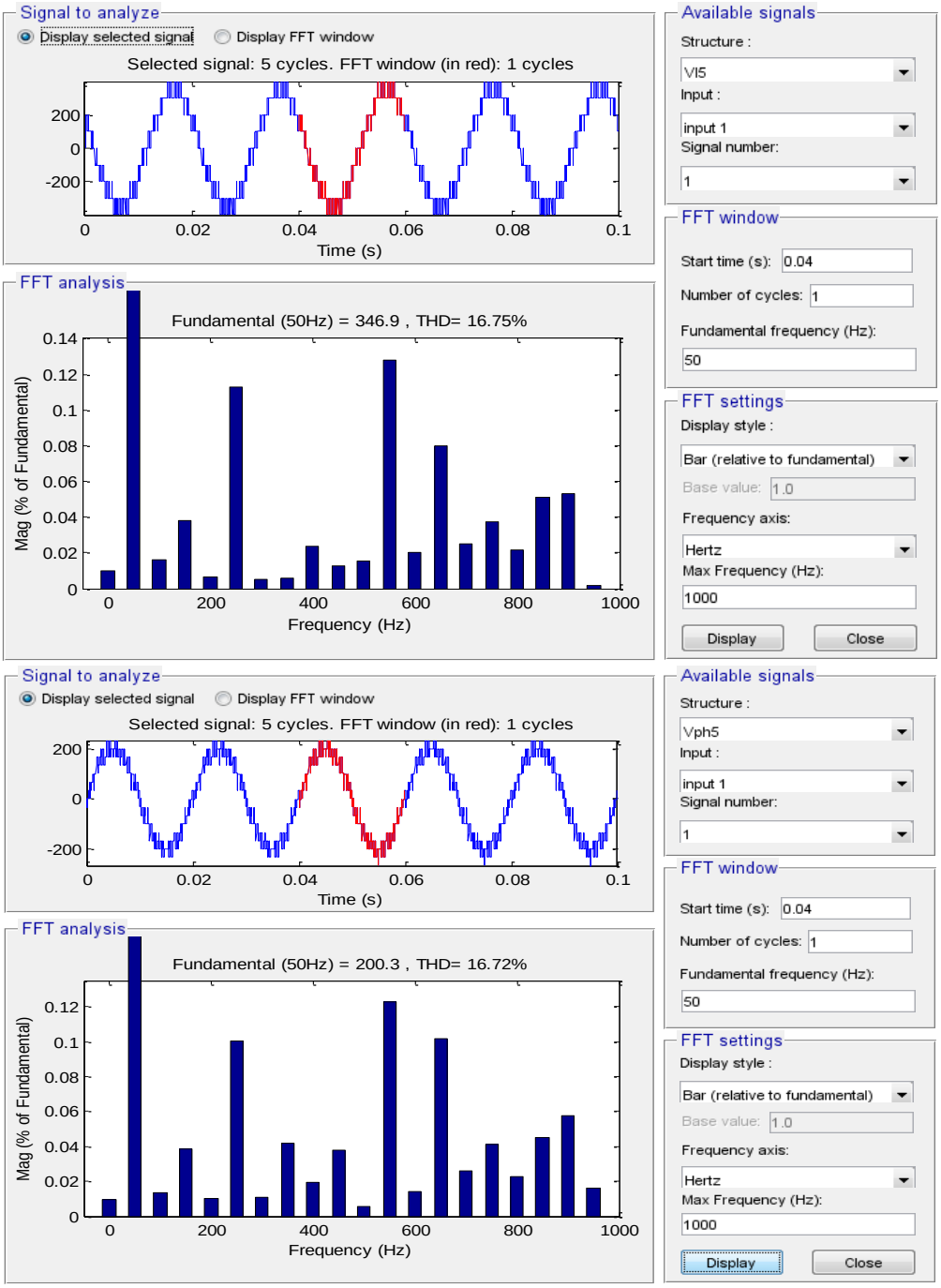


Fig 9: Line and Phase voltage THD analysis

IV. RESULT

Table – 1
Comparison of line and phase voltage THD's for 2-level and multi-level inverters.

LEVEL	% of THD (in line)	% of THD (in phase)
2	61.55	61.51
3	35.86	36.15
5	16.75	16.72

V. CONCLUSION

This project has provided a brief summary of multilevel inverter circuits and their control. However, the commercial products that utilize this superior circuit topology were not available until the mid-1990s. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is going on. This project cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically.

The final THD(Total Harmonic Distortion) results as obtained from the designing, modeling and simulation of different levels of Multilevel Inverters has been represented using waveforms and THD(Total Harmonic Distortion) analysis and have been systematically in the final result table(TABLE 1).

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