Technology and speed are always moving forward day by day, from low scale integration to large and VLSI and from megahertz (MHz) to gigahertz (GHz). The requirements are also rising up with this continuous advancing technology and speed of operation. In synchronous systems, high speed has been achieved using advanced pipelining techniques. Flip Flop (FF) is one of the crucial elements used extensively in all kinds of pipelining techniques. It is estimated that a clock system and a logic part itself consume almost the same power in various chips. That is the clock system consumes 20–45% of the total chip power. The large power consumption of the clock system is due to large transition probability, while the transition probability of the ordinary logic is only one-third of the average. Within the clock system almost 90% of the total power is consumed by the FFs (T. Sakurai and T. Kuroda, 1996). As a result, reduced power consumption by the FF can have a huge impact on the total power consumption of system. In order to reduce the power of the clock system, the voltage swing of the clock should be reduced. Many methods are adopted to reduce the clock swing from earlier times itself (H. Kojima et. al., 1994). But this method came with cost of four clock lines, which in turn increased area overhead and interconnection capacitance. Another reduced clock swing FF is introduced in (H. Kawugachi and T. Sakurai, 1998), using which the clock swing got reduced to 1V, which was a big achievement. Also from a performance perspective, the delay and latency of the FFs consumes a large portion of the cycle time, especially in high operating frequencies.

The FF choice and design can affect both the power dissipation and overall performance of a system. Hybrid Latch FF (HLFF) (H. Patrovi et. al.,1996) and Semi Dynamic FF (SDF) (F. Klass et. al.,1999) are considered as the classic high-performance FFs. They possess a hybrid architecture that combines the merits of dynamic and static structures. In addition, SDF has a distinctive capability of incorporating logic very efficiently because only one transistor is driven by the data input. This greatly helps in reducing the pipeline overhead since the delay and area associated with one or more logic stages preceding the FF can be eliminated. Several modified FF designs have been proposed in the past decade, all aiming at reduction of power, delay, and area. Each FF has its own merits as well as limitations. In semi dynamic FF structures pulses can be used to drive the flip flop instead of clock signals. Depending on the pulse generation method, pulsed flip flops can be classified as implicit or explicit. In an implicit type Pulsed FF (P-FF), the pulse generator is built in to the latch circuit design. There is no need of explicit pulse generator here. In explicit-pulse generator the design of the latch and pulse generator are separate. Since no separate pulse generation techniques are used, implicit flip flops are more power-economical. But they have inferior timing characteristics because of the longer discharging paths in their circuit. The power consumption and complexity of the explicit P-FFs can be reduced by sharing a pulse generator between groups of FFs.
In this paper, chapter 2 gives a detailed description of the existing FF architectures and challenges in achieving high performance. Chapter 3 describes the proposed Conditionally Pulse Enhanced DDFF and its operations. It also explains about incorporating logic into the proposed FF. Section 4 presents the experimental results and findings are concluded in section 5.

II. LITERATURE REVIEW

A. Conventional Flip Flops:

Large numbers of FFs and latches have been published in the past decades. They can be divided into static and dynamic design styles. Static FFs include the conventional master slave design. They dissipate comparatively low power and have a low clock to output (CLK – Q) delay. But the data to output delay (D-Q) is comparatively large in these FFs because of the large set up time. The second category of the FF design, the dynamic FFs includes the modern high performance FFs. There are purely dynamic designs as well as pseudo-dynamic structures. The latter, which has an internal precharge structure and a static output, deserves special attention because of their distinctive performance improvements. They are called the semi-dynamic or hybrid structures, because they consist of a dynamic frontend and a static output.

B. Static Flip Flops:

The Static FFs include the master slave designs, such as the transmission gate based master-slave flip-flop and the PowerPC 603 master-slave latch (S. Gari et al., 1994). They dissipate low power. But the D to Q delay is high because of their large setup time. PowerPC 603 was one of the most efficient classic static structures. It has the advantages of having a low-power keeper structure and a low latency direct path. As mentioned earlier, the large D to Q delay resulting from the positive setup time is one of the limitations of this design. Also, the large data and CLK node capacitances make the design inferior in performance. Despite all these shortcomings, static designs still remain as the low power solution when the speed is not a primary concern. In (G. Gerosa et al., 1994) they made use of this power efficient FF in 2.2V, 80MHz Superscalar RISC microprocessor.

C. Dynamic and Semi dynamic Flip Flops:

The dynamic FFs include the modern high performance FFs. There are purely dynamic designs as well as pseudo dynamic structures. Semidynamic FFs which has an internal precharge structure and a static output, deserves special attention because of their distinctive performance improvements. They consist of a dynamic frontend and a static output. SDFF is shown in Fig. 2.1 and HLFF is shown in Fig. 2.2. These FFs fall under semidynamic category. They benefit from the CLK overlap to perform the latching operation. SDFF is the

![Semidynamic FF (SDFF) (F.Klass Et Al., 1999)](image)

...Fastest classic hybrid structure, but is not efficient as far as power consumption is concerned because of the large CLK load as well as the large precharge capacitance. HLFF is not the fastest but has a lower power consumption compared to the SDFF. HLFF has a single precharge node X driving the output pull up and pull down transistors. When D is HIGH during the overlap period the node X has to discharge through three transistors and there is also a longer stack of nMOS transistors at the output node, making it slower than SDFF and causes large hold-time requirement. This makes the integration of HLFF to complex circuits a difficult process. Also it is inefficient in embedding logic.
The two major sources of power dissipation in the conventional semidynamic designs are the redundant data transitions and large precharge capacitance of the internal node. In order to reduce the redundant data transitions in the FFs many attempts have been made. The conditional discharge flip flop (CDFF) (P. Zhao et al., 2004) employs a technique named conditional discharge. In conditional discharge scheme an nMOS transistor controlled by output feedback is inserted in the discharge path of the stage with high-switching activity. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. As a result, transition at the output switch off the discharge path for first stage to prevent it from discharge and doing evaluation in succeeding cycles as long as the input is holds high. But the major disadvantage of this design is the additional nMOS in the transistor stack. This makes it slower and bulkier. The conditional data mapping FF (CDMFF) (C. K. Teh et al., 2006) is another such FF. This FF uses an efficient technique for reducing the redundant data transitions. It uses an output feedback structure to conditionally feed the data to the flip-flop. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Since there are no added transistors in the pull-down nMOS stack, the speed performance is not greatly affected. But the presence of three stacked nMOS transistors at the output node, similar to HLFF, and the presence of conditional structures in the critical path increase the hold time requirement and D-Q delay of the flip-flop. Also, the additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation.

The next major reason for power dissipation is the large precharge capacitance in the conventional FFs. This is because in most of the conventional design a single internal node is driving the output transistors i.e. both pull up and pull down. These transistors in turn drive large output loads, which also contributes to the capacitance. This common drawback of many conventional designs was considered in the design of XCFF (A. Hirata et al.,2005). The power dissipation is reduced by splitting the dynamic node into two. Each node separately drives the output pull-up and pull-down transistors. Only one of the two dynamic nodes is switched during one CLK cycle. Therefore the total power consumption is considerably low in this FF without any reduction in speed. Major drawbacks of this design are the redundant precharges at internal nodes, requirement of large hold time because of the conditional shutoff mechanism and charge sharing at the internal node. Charge sharing occurs mainly in long discharge paths. When the transistors in the discharge path turns ON when the actual discharge is not needed a dip in the voltage of the internal nodes occurs. This is because of the junction capacitances of the turned ON transistors. This may degrade the voltage level and may cause erroneous transition at the output unless the inverter pair are carefully designed to overcome this. Embedding logic into the FF may result in uncontrollable charge sharing errors.
Another FF named Dual dynamic node pulsed hybrid flip flop (DDFF) (K. Absel et al.,2013) is shown in Fig. 2.3. In DDFF node X1 is pseudo-dynamic in nature. The weak inverter acts as the keeper here. The node X2 is purely dynamic unlike XCFF. Instead of the conditional shut OFF mechanism of discharge path in XCFF, this DDFF has an unconditional discharge path. The redundant precharge at nodes are also eliminated in this design. But the charge sharing problem exists here also. Node X1 undergoes charge sharing when the CLK makes a low to high transition while D is held low. This results in a momentary fall in voltage at node X1. One of the major advantages of the DDFF is the ability to embed complex logic functions into the FF architecture efficiently. It is named as Dual dynamic node pulsed hybrid flip flop with Embedded Logic Module (DDFF-ELM) and is shown in Fig. 2.4. The fact that an N input function can be realized in a positive edge triggered structure using a pull-down network (PDN) consisting of N transistors improves the efficiency in terms of speed and area. The slight change in the clocking scheme makes the charge sharing problem in DDFF-ELM less, which become uncontrollable as the number of transistors increases. One limitation of this DDFF-ELM is the need of the large overlap period because of the long discharge path of internal node. This can be achieved by the use of bulky inverters.

III. ANALYTICAL PROCEDURE

D. Proposed Flip Flop with Pulse Control Scheme:

The proposed conditionally pulse enhanced dual dynamic node FF is shown in Fig. 3.1 The upper part of latch is similar to the one which employed in DDFF design. Instead of the transistor stack design in the discharge path of Fig. 4, transistor NM0 is removed from the discharging path. Transistor NM5 and NM6, which is an additional transistor forms a two input pass transistor logic (PTL) based ‘AND’ gate (Y. H Shu et al.,2006) (P.Zhao et al.,2011). This pass transistor AND controls the discharge of transistor N1. The output node Z is at logic LOW most of the time because the inputs to the AND logic are clock and it’s complimentary. The AND logic gives a HIGH only during the transition edge of the clock. At the rising edges of the clock, when both the transistors NM5 and NM6 are turned ON a weak logic HIGH is passed to the node Z. It turns ‘ON’ the transistor NM2. This happens only for a small time determined by the inverter INV5. The reduced voltage swing
results in reduced switching power at node Z. Also the discharging path contains reduced number of stacked transistors. As a result of this reduced number of transistors, the time to discharge the node X is less. I.e. the delay gets reduced.

In this design, the longest discharging path occurs when input data are 1. A transistor PM3 is added in order to enhance the discharge under this condition. Transistor PM3 is normally turned OFF because node X1 is HIGH most of the time. Only when node X1 is discharged to [VTP], the transistor PM3 turns ON. This provides additional boost to node Z (from VDD-VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor NM2.

The voltage level of node X1 rises during precharge and turns off transistor PM3 eventually. A large pulse gets generated giving enough time to correctly capture the data only when it is needed. The bulky delay inverter in the DDFF and DDFF-ELM which consumes large power during pulse generation can be avoided. The leakage power also gets reduced because of the smaller transistors in the discharge path and in the delay inverter. Also the problems of charge sharing decreases as the number of transistors in the discharge path are less.

The working of Flip Flop is as follows. The latching of the data occurs only when the pulse is high. If the input is high prior to the pulse generation then node X1 is discharged through NM1-2 i.e. only through two transistors whereas it was three in case of DDFF resulting in a faster discharge. Also the generated pulse at this instant will be larger because node X1 turns ON transistor PM3 which pulls up the pulse to a strong ‘HIGH’. This switches the state of the cross coupled inverter pair INV1-2. Causing node X1B to go high and output QB to discharge through NM4. The node X2 is held high by the pMOS transistor PM1. As the pulse falls low, the circuit enters the precharge phase and node X1 is pulled high through PM0, switching the state of INV1-2.

During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If D is zero prior to the pulse, node X1 remains high. The pulse generated during this time will have less voltage swing resulting in low power dissipation. Since X1 remains HIGH node X2 is pulled low through NM3 as the pulse goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the pulse falls low, node X1 remains high and X2 stores the charge dynamically. The architecture exhibits negative setup time since the short transparency period defined by the l–l overlap of CLK and CLKB, that is the pulse width allows the data to be sampled even after the rising edge of the CLK before CLKB falls low.

E. Embedded Logic Module:

Incorporating logic into FFs is somewhat difficult. SDFF is the capability to incorporate complex logic functions efficiently. By incorporating logic to the FF the area as well as delay can be reduced to a larger extent. The pipeline overhead of the whole circuit gets eliminated. Even though SDFF is capable of incorporating logic functions, the power consumed by this circuit is very large. In DDFF-ELM even though the charge sharing problem in SDFF is eliminated by the clock rearrangement, it requires a larger overlap period which is achieved by the use of bulky inverters. Charge sharing becomes uncontrollable as the number of transistors in the stack increases. For reducing this effect we have to decrease the number of transistors in the stack. By adopting conditional pulse enhancement mechanism we can achieve shorter discharge path as well as larger pulses only when the logic output needs to be HIGH.

Fig. 3.2 shows the design of the proposed Conditionally Pulse Enhanced DDFF-ELM AND. A two input AND is embedded to the FF. The two inputs A and B get evaluated according to their values when the pulse is high. Here the longest discharge path consists of three transistors only and it occurs when A = B = 1 and pulse becomes high. Then the three transistors NM0-2 gets turned ON and PM3 pulls up the node Z and we get a sufficiently large pulse in order to latch the value of the logic to the output. In all other cases i.e. A = 0 and B = 1, A = 1 and B = 0, A = B = 0, PM3 remains OFF and we get pulses with low voltage swing resulting in less power dissipation.

Fig. 3.3 shows the proposed Multiplexer Embedded Conditionally Pulse Enhanced DDFF. The four inputs are A, B, SEL_A and SEL_B. It implements the function A.SEL_A + B.SEL_B. When SEL_A becomes high the multiplexer selects the value of input A and when the pulse comes FF latches this particular value to the output. Here the longest discharge path consists of three transistors only and it occurs when A = SEL_A = 1, B = SEL_B = 1 and pulse becomes HIGH. Then PM3 pulls up the node Z and we get a sufficiently large pulse in order to latch the value of the logic to the output. In all other cases PM3 remains OFF and we get pulses with low voltage swing resulting in less power dissipation.
IV. RESULTS AND DISCUSSION

In order to understand the effectiveness of the proposed design, the performance of the proposed FF design is evaluated against the existing design. The compared designs include SDFF, HLFF, DDFF and DDFF-ELM. The Pyxis schematic of Mentor Graphics is used in order to create the schematics of the circuit. The performance of the pulse enhanced P-FF design is evaluated against existing designs through pre-layout simulations using eldo simulator. The output waveforms are viewed using E-Z wave viewer. The target technology is the TSMC 180-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width. The operating condition used in simulations is 500 MHz/1.8V. In order to analyze the power consumption data pattern with 50% transition probability is given at a temperature of 27°C.

A. Output Waveform of Proposed FF:

Fig. 4.1 shows the waveform of the proposed FF. We can see that pulses get generated on the each rising edge of the clock. Only when V(D) is ‘HIGH’ the generated pulses are large. Only during this time the actual pull down is needed. These width and height enhanced pulses increases the pull down strength and faster discharge occurs. The power is also maintained low since the size of the pulses in all other cases are small with reduced voltage swing. When V(D) is LOW the pulses are of small width and height making it more power efficient.
B. Output Waveform of Proposed FFs with Embedded Logic Module:

Fig. 4.2 and Fig. 4.3 show the output waveform of Proposed Conditionally Pulse Enhanced DDFF-ELM AND and MUX. It is evident from the waveforms that only when the output needs a transition from ‘LOW’ to ‘HIGH’ an enhanced pulse gets generated. In all other cases pulses with low voltage swing are generated. In the case of ‘AND’ logic only when both the inputs are ‘HIGH’ we are getting an enhanced pulse. Similarly when select signal and input are high an enhanced pulse gets generated.
Table 4.1 illustrates the speed and power delay product (PDP) of various flip-flops at 50% data activity. The results show that the proposed flip-flops have the lowest power dissipation among the group. The transistor count remains almost same for all the flip flops. Also the D-Q delay is also less compared to other Flip Flops.

<table>
<thead>
<tr>
<th>Flip Flops</th>
<th>No. of transistors</th>
<th>D-Q Delay (pS)</th>
<th>Total Power (pW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDFF</td>
<td>23</td>
<td>213</td>
<td>392.98</td>
</tr>
<tr>
<td>HLFF</td>
<td>20</td>
<td>216</td>
<td>347.25</td>
</tr>
<tr>
<td>DDFF</td>
<td>18</td>
<td>204</td>
<td>326.38</td>
</tr>
<tr>
<td>DDFF-ELM</td>
<td>23</td>
<td>229</td>
<td>328.92</td>
</tr>
<tr>
<td>Proposed FF</td>
<td>20</td>
<td>194</td>
<td>309.37</td>
</tr>
<tr>
<td>Proposed FF-ELM</td>
<td>21</td>
<td>198</td>
<td>310.82</td>
</tr>
</tbody>
</table>

The Table 4.2 gives a detailed comparison of DDFF to the proposed Conditionally Pulse Enhanced DDFF. The results show that the proposed flip flop gives 9.8%, 18.2%, and 18.7% reduction in Power Delay product (PDP) compared to DDFF, Embedded AND logic, and Embedded 2x1 MUX logic respectively. This shows that the power as well as the speed of the proposed FF is improved.

Table 4.2 Performance comparison of DDFF and proposed FF

<table>
<thead>
<tr>
<th>Logic Functions</th>
<th>DFF</th>
<th>Proposed FF</th>
<th>∆PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Power Dissipated (pW)</td>
<td>D to Q Delay (ns)</td>
<td>Power Dissipated (pW)</td>
</tr>
<tr>
<td>FF</td>
<td>326.38</td>
<td>0.204</td>
<td>309.37</td>
</tr>
<tr>
<td>AND Logic</td>
<td>328.92</td>
<td>0.229</td>
<td>310.82</td>
</tr>
<tr>
<td>2 x 1 MUX</td>
<td>344.44</td>
<td>0.230</td>
<td>315.38</td>
</tr>
</tbody>
</table>

V. CONCLUSION

The clock system (FF modules) of a circuit consumes nearly half of the total power. Therefore reducing the power of clocking elements can reduce the total power consumption of the system. The choice of the flip flop design has a huge impact on the power consumption as well as performance of the system. Here, a Conditionally Pulse Enhanced DDFF is proposed. Proposed FF is capable of effectively incorporating logic to the FF also. The conditional pulse enhancement scheme consists of a simple two transistor pass transistor ‘AND’ gate design. The conditional pulse enhancement scheme reduces the number of transistors stacked along the discharging path and it supports conditional enhancement of the height and width of the discharging pulse. So the size of the transistors in the pulse generation circuit can be kept to minimum. A comparison of the proposed flip-flop with the conventional flip-flops showed that it exhibits lower power dissipation along with comparable speed performances. The simulation results show that the proposed FF gives 9.8%, 18.2%, and 18.7% reduction in Power Delay product (PDP) compared to DDFF, DDFF-ELM AND, DDFF-ELM MUX. The proposed architectures can be used for design of sequential circuits where area, delay-overhead and power dissipation are of major concern.

REFERENCES


