Comparative Study of Silicon and Germanium Doping-less Tunnel Field Effect Transistors

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Abstract

An alternative to conventional field effect transistors Tunnel Field Effect Transistor (TFET) provides a very steep sub threshold slope and low leakage current. Doping less Silicon TFET avoids certain challenges faced by TFET like effects of Random Dopant Fluctuations (RDF), like an unacceptably large increase in the OFF-state current and need of high temperature for doping process and related process like ion implantation and annealing techniques during its fabrication. The performance of the device can be improved by using various performance boosters such as material engineering, barrier engineering, gate stack engineering, structural engineering etc.

Keywords: Band to band tunnelling, charge plasma, Double gate, high-k dielectric, Tunnel Field Effect Transistor

I. INTRODUCTION

The need for higher computing power at cheaper cost results in continuing CMOS scaling. Device scaling allows for more devices and/or functions to be integrated into a single chip. MOSFET device scaling plays an important role in the rapid development of the semiconductor industry. MOSFETs have also been greatly miniaturized [1]. Scaling of Si MOSFET is faced with several problems. This situation results in looking towards alternatives to the conventional bulk silicon MOSFET by exploring new materials as well as new device architectures as replacement or add-ons to the current CMOS technology. Some of the limitations faced by MOSFET are the power consumption, leakage current, subthreshold swing limitation, short channel effects etc. In order to reduce the power consumption, the supply voltage has to scale down. This results in the reduction in threshold voltage to maintain the device performance. As a result the off state current increases. Theoretically MOSFET subthreshold swing (SS) is limited to 60mV/decade. Practically SS is greater than 60mV/decade. Tunnel field effect transistor is one of the alternative structures to overcome the conventional FET limitations. The tunneling phenomenon was introduced in semiconductor devices to overcome the thermal voltage limitation of the conventional FETs. BTBT devices have the potential to offer subthreshold swing below 60mV/decade (at room temperature) since they are independent of the thermal voltage (KT/q) [2].

TFET exhibits an extremely low SS value and its ON/OFF current ratio is lower than that of the conventional MOSFETs. The low ON current stems from the difference of carrier injection mechanisms between the TFET and the MOSFET. It is well known that the band-to-band tunneling current becomes less sensitive to the electric field as the potential difference between the channel and the source increases. Some of the approaches for further improvement in the ON current are the use of lower bandgap material, lower equivalent oxide thickness (EOT), and a more abrupt source doping profile [2]. The lower bandgap material can be used in the entire active device area or only in the selected region where the band-to-band tunneling occurs. TFETs in general suffer from low ON-state current (ION). The other problem with the TFET is the effects of random dopant fluctuations (RDF), such as an unacceptably large increase in the OFF-state current. The presence of doped source and drain needs a complex thermal budget for ion implantation and expensive thermal annealing techniques [3]. Creating abrupt junctions that are essential for efficient tunneling using high temperature processes is not easy due to the diffusion of the dopant atoms from the source/drain regions into the channel. This paper introduces a new structure for TFET to overcome these limitations. The proposed device is doping-less Ge tunnel field effect transistor (TFET). It is based on the charge plasma concept. Without the
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This paper is organized into 5 sections. Section 2 introduces the TFET and its working principle. Section 3 and 4 introduces silicon Doping less TFET and germanium Doping less TFET. Section 5 deals with the analysis and comparison of Si and Ge Dopingless TFET and the observations obtained. Finally last section concludes the paper.

II. TFET

Tunnel Field Effect Transistor (TFET) is an emerging trend in semiconductor devices based on Band-to-Band tunneling mechanism has a very strong potential to overcome the thermodynamic barrier of conventional FETs and provide a very steep sub threshold slope. Tunnel FETs are gated p-i-n diodes or, less common, p-n junctions. The gate runs along the entire intrinsic region in the case of a p-i-n structure. The gated structure is shown in Fig.2.1 together with the band diagram in the off state. It is a p-type device with the n+ doped part being the source and the p part the drain. At negative VDS and zero gate voltage current is suppressed by the barrier at the source, channel and drain regions. This results in very low off-state leakage currents [5]. If a negative gate voltage is applied, such that the valence band edge in the channel is pushed above the conduction band edge at the source, holes are injected into the channel via BTBT and constitute a drain current Id as in the case of an Esaki diode as shown in (blue arrow) Fig.2.2.

During the BTBT process the energy gaps of the n+-doped and the gated region of a Tunnel FET act as energy filters, and thus high energetic carriers in the Fermi distribution are suppressed in the current flow. This is depicted by the small energetic window $\Delta \phi$s through which only carriers can tunnel through. By eliminating the high energetic tail of the Fermi distribution, the electronic system gets effectively “cooled down”, i.e. the entire system acts like a conventional MOSFET at a lower temperature [5]. This is the reason why in principle, BTBT current can achieve $S$ values smaller than 60 mV/decade.

The tunneling current depends on the transmission probability, $T(E)$ of the inter-band tunneling barrier. To describe the BTBT current and get an overview on device parameters which influence the performance, the tunneling probability at the junction has to be considered. The BTBT current is proportional to the tunneling probability which can be approximated by the Wenzel-Kramer-Brillouin (WKB) method [3] as given in equation (2.1)
\[ I = \frac{4q}{\hbar} \int T(E) \left[ f_S(E) - f_D(E) \right] dE \quad (2.1) \]

where \( T(E) \) is the transmission probability across the junction, \( f_S(E) \) and \( f_D(E) \) are the fermi function in the source and the drain respectively, \( q \) is the electron charge, and \( \hbar \) is the Planck's constant and tunnel probability, \( T(E) \) is given by the equation (2.2).

\[ T(E) = e^{-\frac{4}{3\pi q \xi^2} \left( \frac{2m^*E_g^2}{q^2\xi^2} \right)} \quad (2.2) \]

where \( m^* \) is the effective carrier mass, \( E_g \) is the band gap, \( h \) is the Dirac Planck’s constant , \( h = \hbar/2\pi \). \( \xi \) can be expressed as shown in the equation (2.3).

\[ \xi = \frac{\Delta \phi + E_g}{\lambda} \quad (2.3) \]

where \( \lambda \) is the screening length and \( \Delta \phi \) denotes the energy overlap between the conduction band edge and the valance band edge at the source/channel tunneling junction[4].

The screening length \( \lambda \) refer to the spatial extent of the electric field, which depends on the device geometry (number of gates), the dielectric constants and the thickness of the gate dielectric and semiconductor used in the device. Increasing the number of gates will reduce the screening length. The tunneling arises through the screening length. As the channel length scaled down the depletion zones of the source and drain side cross. The barrier is reduced and the source drain potential contributes to band bending over a significant portion of the device and the rest of charge controlled by the gate. A small screening length will reduce the drain contact on the channel and suppresses short channel effect (SCE). \( \lambda \) depends on device geometry, doping profiles, and gate capacitance. Screening length should be minimized for high barrier transparency [4,5]. One of the challenges in Tunnel FETs is to achieve high enough on-currents. Because only a limited number of states within the energetic window constitute to the tunneling, the current of a Tunnel FET is generally lower than that of a MOSFET. For high current \( T(E) \) close to unity and for that screening length is as small as possible.

### III. Silicon Doping-less TFET

Silicon Doping-less TFET is lateral p-i-n structure and it is simulated using Sentaurus TCAD tool. The simulation structure of the Silicon Doping-less TFET is shown in fig: 3.1. Intrinsic silicon is used as the source, channel and drain regions. In the doping-less TFET, the “p” source and “n” drain regions are formed using the charge plasma concept [7, 8]. Source and drain regions are formed on the intrinsic material as p type and n type by inducing carriers. Doping and its related processes are not needed for these region formations. Channel length of 50nm is used. Inducing carriers in the regions is by selecting proper metals as electrodes. That means metal electrodes having proper work function which satisfies the equation 4 and 5. Under thermal equilibrium conditions, for creating the “n” drain region by inducing electrons with a concentration similar to the N+ drain doping of the reference device in the intrinsic silicon body, hafnium (work function=3.9 eV) is employed as the drain metal electrode [6]. Similarly, for creating the “p” source region by inducing holes with a concentration similar to the P+ source doping of the reference device in the intrinsic silicon body, platinum (work function = 5.93 eV ) is employed as the source metal electrode.

![Fig: 3.1: Simulation structure of Silicon Doping less TFET](image)

There are two essential features in this concept. First, the work functions of the gates should be different from that of silicon [7]. For p type formation or hole plasma in a region, the metal to be used as the contact of this region should satisfies the equation (3.1).

\[ \varphi_{M1} > \chi_{Si} + \frac{E_g}{2} \quad (3.1) \]

Similarly to create electron plasma in drain, the work function of drain metal electrode must be satisfying the condition shown in equation (3.2). \( \chi_{Si} \) is the electron affinity of silicon, \( E_g \) is the band gap of silicon.

\[ \varphi_{M2} < \chi_{Si} + \frac{E_g}{2} \quad (3.2) \]

Band gap of Si is 1.11eV and electron affinity is 1.3895210(7) eV. \( \varphi \) is the work function of the metal electrode. To maintain uniform induced carrier distribution throughout the silicon thickness in the source and drain regions, from the oxide-Si interface to the Si-buried oxide interface along the Y-direction, the silicon film thickness has to be kept within the Debye length,
\[ L_D = \sqrt{\frac{\varepsilon_{si} V_T}{qN}} \quad (3.3) \]

where \( \varepsilon_{si} \) is the dielectric constant of silicon, \( V_T \) is the thermal voltage, and \( N \) is the carrier concentration in the body [8]. The ON current can be improved by using strain, high-k dielectric, and narrow bandgap materials such as germanium or hetero structures.

IV. GERMANIUM DOPING LESS TFET

To improve device characteristics, the Germanium Doping-Less TFET merges the two emerging trends in material and device structure to increase the drain to source current of the tunneling devices. BTBT mechanism is used the TFET device and band gap is regarded as barrier potential. Tunneling probability as shown in equation (2) is indirectly proportional to the bandgap (\( E_g \)) of materials. So smaller band gap materials can improve tunneling probability and thereby increase the on-state current.

In Ge Doping-less TFET by using Germanium materials will indicate that at junction side the minimum band gap has been made and the high ON current can been obtained. Multi-gate would result in better gate modulation of TFETs, enhancing BTBT, improving the tunneling current. In these TFET using charge plasma concept is free from doping and related processes like ion implantation, annealing etc. Thereby it requires low thermal budget for its fabrication. To improve device characteristics the proposed TFET merges the two emerging trends in material and device structure. This paper proposes a TFET structure to increase the drain to source current of the tunneling devices. Effect of material on the device performance has recently been considered.

In proposed TFET by using Germanium materials will indicate that at junction side the minimum band gap has been made and the high ON current can been obtained. Multi-gate would result in better gate modulation of TFETs, enhancing BTBT, improving the tunneling current. Fixing the gate work function to an optimum value is also technique for improvement of \( I_{ON} \).

Usage of high-k material like HfO\(_2\) in place of SiO\(_2\) will also improve the performance of TFET. An improved on-current and low subthreshold swing can be achieved by the proper choice of a gate dielectric. The gate dielectric constant increases as high-k dielectrics provide better gate coupling [9]. As TFETs working principle is gate modulated BTBT, the gate control over the channel surface is an important factor determining the device performance.

![Fig. 4.1 Simulation Structure Of Germanium Doping Less TFET](image)

The simulation structure is shown in fig. 4.1. Gate length is taken as 50nm. Thickness of Germanium is taken as 10nm. So quantum mechanical effects are not considered. Germanium is used as source, channel and drain material. The entire active region (source-channel-drain) of the device is separated from the body by a buried layer of high k material. HfO\(_2\) is used as dielectric material. We have inserted 3nm thick HfO\(_2\) between the germanium and gate electrode. Nitride is used as spacer oxide. And also 3nm thick HfO\(_2\) between the germanium and drain metal electrode. Simulation of the structure of Ge Doping-less TFET is performed using Sentaurus TCAD.

Gate metal electrode is Aluminum. As satisfying the condition shown in equation (4.1) and (4.2) Platinum is used as source metal electrode and Titanium is the drain metal electrode. In order to create hole plasma in source, the work function of source metal electrode must be satisfy the following condition as shown in equation (4.1). \( E_g \) is the bandgap and \( \chi_{Ge} \) is the electron affinity of the material used in source region. Band gap of Ge is 0.66 eV. And electron affinity is 1.2326744(12) eV.

\[ \Phi_{M1} > \chi_{Ge} + \frac{E_g}{2} \quad (4.1) \]
\[ \Phi_{M2} < \chi_{Ge} + \frac{E_g}{2} \quad (4.2) \]

Similarly to create electron plasma in drain, the work function of drain metal electrode must be satisfying the condition as shown in equation (4.2). \( E_g \) is the bandgap and \( \chi_{Ge} \) is the electron affinity of the drain material.
V. ANALYSIS AND OBSERVATIONS

In this paper a detailed study of the Silicon Doping less TFET and Germanium Doping less TFET are to be performed. Without the need for any doping process, the source and drain regions are formed using the charge plasma concept by selecting appropriate work functions for the source and drain metal electrodes. It requires low thermal budget for its fabrication. Simulation of these doping less TFET is performed using Sentaurus TCAD. We can understand that the drain and source regions formed on the intrinsic materials are expected to be similar to the conventional TFETs. The subthreshold swing is defined as the amount of gate voltage necessary to increase or decrease the subthreshold drain current by a factor of 10, usually expressed in millivolts per decade (mV/decade). The subthreshold swing is calculated by using the equation 5.1.

\[ SS_{avg} = \frac{(V_{T} - V_{OFF})}{\log(I_{OFF}) - \log(I_{OFF})} \]  

(5.1)

The transfer characteristics of the Silicon Doping-less TFET are shown in fig. 5.1. The \( I_{D} - V_{GS} \) curve is plotted for the values of \( V_{DS} \) at 0.3V. Corresponding log \( I_{D} - V_{GS} \) graph is shown in the fig. 5.1. The OFF state current of Heterojunction Doping-less TFET is as low as \( 1 \times 10^{-12} \) A/µm and the ON state current of Heterojunction Doping-less TFET is \( \sim 1.1 \times 10^{-8} \) A/µm. The \( I_{ON} \cdot I_{OFF} \) ratio is \( 10^4 \). The subthreshold swing of the Silicon Doping-less TFET is calculated by using the equation (5.1) and is 74.23mV/decade.

The transfer characteristics of the Germanium Doping-less TFET are shown in figure 4.5. The corresponding log \( I_{D} - V_{GS} \) graph is shown in the figure 4.6. The ON state current of Ge Doping-less TFET is \( \sim 1 \times 10^{-5} \) A/µm as shown in figure. The OFF state current of Ge Doping-less TFET is \( \sim 1 \times 10^{-10} \) A/µm. And thereby ON-OFF ratio is approximately \( 10^5 \). The subthreshold swing is calculated by using the equation (5.1). The SS of Ge Doping-less TFET is 60 mV/decade. The performance comparison of Si and Ge dopingless TFETs are shown in table 5.1. The ON current and switching ratio is better for Ge dopingless TFET as compared with Si dopingless TFET.

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**Fig. 5.1: \( I_{D} - V_{GS} \) And Log\( I_{D} - V_{GS} \) Of Silicon Dopingless TFET**

**Fig. 5.2 \( I_{D} - V_{GS} \) And Log\( I_{D} - V_{GS} \) Of Germanium Dopingless TFET**
<table>
<thead>
<tr>
<th></th>
<th>$I_{ON}$ (A/μm)</th>
<th>$I_{OFF}$ (A/μm)</th>
<th>$I_{ON}/I_{OFF}$ Ratio</th>
<th>SS (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Doping less TFET</td>
<td>$1.1 \times 10^{-8}$</td>
<td>$1 \times 10^{-12}$</td>
<td>$1.1 \times 10^{4}$</td>
<td>74.23</td>
</tr>
<tr>
<td>Germanium Doping less TFET</td>
<td>$1 \times 10^{-7}$</td>
<td>$1 \times 10^{-10}$</td>
<td>$1 \times 10^{7}$</td>
<td>60</td>
</tr>
</tbody>
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VI. CONCLUSION

TFET is one of the emerging trends that overcome the drawbacks of conventional MOSFETs. Even if TFET provides low subthreshold swing and low off state current, it faces several limitations like low on state current and RDF effects. RDF effects, need of highly expensive annealing process, high thermal budget for the doping and the abrupt junction formation can be avoided by the proposed Doping less Ge TFET. The proposed structure combines the advantages of material and double gate TFET technology. The on state current can be improved by using smaller band gap material in the source side and using a double gate structure. Results in improved the ratio of ON current to OFF current. Source and drain are formed without the doping process eliminates the high temperature doping and expensive annealing process during its fabrication. Further improvements can be obtained by using heterojunction of III – V compounds as materials.

REFERENCES