Stage Control unit for Indigenous Processor Based System

Priyanka Rajendran
Department of Electronics and Communication
Toc H Institute of science and technology
Ernakulam, India

Dr. Gnana Sheela .K
Department of Electronics and Communication
Toc H Institute of science and technology
Ernakulam, India

Abstract

Vikram 1601 is an indigenous processor based system for acquisition of stage parameters of launch vehicles, processing of stage parameters and issuing of commands based on the inputs. It can independently execute algorithms related to stage management, thus offloading mission computer from the related tasks. The peripherals of VIKRAM 1601 is ADC (AD7876),DAC (AD664),Multiplexer (HI 506 A),input signal processing circuits, memory, Data acquisition and controlling of OBC is very important. So along with the controller it can it can support both the data acquisition and controlling of vikram 1601. The AD 7876 are fast,complete,12-bit analog to digital converters (ADCs). These converters consist of a track-and-hold amplifier, an 8 micro second successive approximation ADC ,a 3 V buried zener reference, and versatile interface logic. The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data read back function. All DAC read and write operation occur through a single microprocessor-compatible I/O port.2K X 16 memory. Stage parameters are the input for the signal processing circuits. The control unit is designing using VHDL language and testing can be performing using Actel FPGA board.

Keywords: VIKRAM 1601, stage parameters, cro & semi cryo-stage, FPGA, Zener reference, data acquisition, On board computer(OBC)

I. INTRODUCTION

Launch vehicle has different stages solid, liquid , cryo and semi-cryo . Controlling of these stage parameters and processing of stage parameters and issuing of commands based on the inputs. It can be done by using processor based system. It can independently execute algorithms related to stage management, thus offloading mission computer from the related tasks. A multistage (or multi-stage) rocket is a rocket that uses two or more stages, each of which contains its own engines and propellant. Two-stage rockets are quite common, but rockets with as many as five separate stages have been successfully launched. This staging allows the thrust of the remaining stages to more easily accelerate the rocket to its final speed and height. In olden days the controlling of these stages are done by FPGA based systems but it is not applicable for cryo and semi-cryogenics because FPGA can’t execute complex algorithms. The first processor that is used for stage control and processing is Motorola 68000/68000. The 68000 grew out of the MACSS (Motorola Advanced Computer System on Silicon) project, begun in 1976 to develop an entirely new architecture without backward compatibility. It would be a higher-power sibling complementing the existing 8-bit 6800 line rather than a compatible successor. In the end, the 68000 did retain a bus protocol compatibility mode for existing 6800 peripheral devices, and a version with an 8-bit data bus was produced. However, the designers mainly focused on the future, or forward compatibility, which gave the 68000 platform a head start against later 32-bit instruction set architectures. For instance, the CPU registers are 32 bits wide, though few self-contained structures in the processor itself operate on 32 bits at a time. But Motorola 68000 can’t use for processing complex algorithms and it doesn’t support floating point arithmetic. So moved to Intel 960 processor.

Intel 960 processor was a RISC-based microprocessor design that became popular during the early 1990s as an embedded microcontroller, becoming a best-selling CPU in that field. In spite of its success, Intel dropped i960 marketing in the late 1990s as a side effect of a settlement with DEC in which Intel received the rights to produce the StrongARM CPU. The processor continues to be used in a few military applications. The demise with the Intel 960 processor is, Intel attempted to bolster the i960 in the I/O device controller market with the I2O standard, but this had little success and the design work was eventually ended. The ultimate problem is that Intel 960 processor is embargoliste.Cryogenics in itself invites challenges like handling fluids at low temperature under high pressure. So, an efficient pressure measurement system is demanded for monitoring cryo-fuel tank pressures. In our indigenous Cryo stage, Liquid Oxygen (LOX) and Liquid Hydrogen (LH2) are used as propellants. Right from filling of propellants into the fuel tanks, till the end of the mission, the pressure inside the fuel tanks are to be monitored carefully. This measurement is mission critical and it calls for a fault tolerant pressure measurement system with necessary communication links to the OBCs and to the telemetry system.

This project aims design and development of a stage control unit for indigenous processor (VIKRAM 1601 ) based system. New missions requires complex algorithms to be executed along with the stage parameters. This can be done using a processor so old FPGA based system is modified with processor (VIKRAM 1601). For the first time, use of indigenous designed and
developed On-Board computer (OBC) with Vikram 1601 processor in both primary and redundant chains of the vehicle. The OBC performs the functions of Navigation, Guidance and Control processing for the vehicle. The processor based system consists of indigenous processor (VIKRAM 1601) and peripherals. The peripherals of VIKRAM 1601 is ADC (AD 7876), DAC (AD 664), Multiplexer (HI 506A), input signal processing circuits, memory. The AD7876 are fast, complete, 12-bit analog-to-digital converters (ADCs). These converters consist of a track-and-hold amplifier, an 8 μs successive approximation ADC, a 3 V buried Zener reference, and versatile interfacelogic. The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port. The internal memory of vikram 1601 is 2K x 16 bit A control unit (CU) handles all processor control signals. It directs all input and output flow, fetches code for instructions from micro programs and directs other units and models by providing control and timing signals. A CU component is considered the processor brain because it issues orders to just about everything and ensures correct instruction execution. Stage parameters are the input for the signal processing circuits. The control unit is designing using VHDL language and testing can be perform using Actel FPGA board.

II. PROBLEM DEFINITION

Earlier generation OBC used FPGA, Motorola 6800/68000, Intel 960 based processors for performing navigation, guidance and control related computation tasks whereas the current system for ISRO launch vehicle uses indigenous Vikram 1601 processor with dual redundant 1553 bus. The OBC is designed with built-in self test capability for detecting the internal failure. The different application tasks are scheduled in minor (2011s) and major (500ns) cycle periodicity in the OBC. Currently the computational margin available in 20 ms periodicity for current satellite launch vehicles is the order 3-4ms whereas for planned reusable missions it is merely 1 Ms. A new approach is proposed to use Vikram 1601 processors in a single board which allows more computational margin/slack time for further computational requirement. The onboard computer (OBC) is the brain in the autonomous control of the launch vehicle and it aims for secure data transmission to the various remote modules in the system configuration.

A. Goals And Objectives

Fourth generation OBC must be designed to provide services for future space transportation system with better long term reliability features. The goal is to achieve high processing speed and fault tolerant system with the currently available indigenous processor ‘Vikram 1601’. Control of this processor and peripherals are very important. A control unit (CU) handles all processor and peripherals control signals. It directs all input and output flow, fetches code for instructions from micro programs and directs other units and models by providing control and timing signals. A CU component is considered the

III. METHODOLOGY

CUs are designed in two ways:

1) Hardwired control: Design is based on a fixed architecture. The CU is made up of flip-flops, logic gates, digital circuits and encoder and decoder circuits that are wired in a specific and fixed way. When instruction set changes are required, wiring and circuit changes must be made. This is preferred in a reduced instruction set computing (RISC) architecture, which only has a small number of instructions.

2) Microprogram control: Microprograms are stored in a special control memory and are based on flowcharts. They are replaceable and ideal because of their simplicity.

A. Vikram 1601

The ASIC Onboard Computer is based on indigenously developed VIKRAM 1601 processor. It is a 16-bit microprocessor. This processor is built specifically for ISRO Launch Vehicle applications. Since this OBC has its own unique instruction set, all software development tools like Vikram Ada Compiler (VAC), Assembler (VASM), Linker (VLINK), System Generator (VSYS), Simulator (VSIM), Real Time Executive (REX) and all the library Routines have been developed in house. The instruction set has 96 instructions including those for floating point arithmetic. This processor supports 2 addressing modes.
Processor (Vikram 1601) based system for acquisition of stage parameters of launch vehicles, processing of stage parameters & issuing of commands based on the inputs. In-circuit programmability possible. It can independently execute algorithms related to stage management, thus offloading mission computer from the related tasks (e.g., cryo & semi-cryo algorithms, sequencing etc). Complex sequencing possible. Error handling made simpler by tight synchronization with OBC. A single system can be qualified for OBC also (Dual use feature). Implementation with indigenous components as far as possible. (*Vikram 1601* to be used as processor, ‘Protocol Controller ASIC’ to be used for 1553 bus handling etc) FPGA obsolesce taken care in design.

**B. Peripherals Of OBC**

1) **AD 7876 Analog To Digital Converter**

The AD7870/AD7875/AD7876 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8 ms successive approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required. The parts offer a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors. All parts operate from ±5 V power supplies. The AD7870 and AD7876 accept input signal ranges of ±3 V and ±10 V, respectively, while the AD7875 accepts a unipolar 0 V to +5 V input range. The parts can convert full power signals up to 50 kHz. The AD7870/AD7875/AD7876 feature dc accuracy specifications such as linearity, full-scale and offset error. In addition, the AD7870 and AD7875 are fully specified for dynamic performance parameters including distortion and signal-to-noise ratio. The parts are available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP). The AD7870 and D7875 are available in a 28-pin plastic leaded chip carrier (PLCC), while the AD7876 is available and in a 24-pin small outline (SOIC) package.
2) **HI 506A Multiplexer**

The HI-506/HI-507 and HI-508/HI-509 monolithic CMOS multiplexers each include an array of sixteen and eight analog switches respectively, a digital decoder circuit for channel selection, voltage reference for logic thresholds, and an enable input for device selection when several multiplexers are present. The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch up. DI also offers much lower substrate leakage and parasitic capacitance than conventional junction isolated CMOS (see Application Note AN520). The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic “1” and maximum 0.8V for logic “0”. This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. The HI-506 is a single 16-channel, the HI-507 is an 8-channel differential, the HI-508 is a single 8-channel and the HI-509 is a 4-channel differential multiplexer. If input overvoltage is present, the HI-546/HI-547/HI-548/ HI-549 multiplexers are recommended.

![Fig. 2: pin diagram of AD 7876](image1.png)

C. **AD 664 DAC**

The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port. The I/O port accommodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data. The analog portion of the AD664 consists of four DAC cells, four output
amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference. The functional completeness of the AD664 results from the combination of Analog Devices’ BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

Fig. 4: Block Diagram For Stage Controller For Vikram 1601

Fig. 5: State Diagram for Controlling the Data Acquisition System
IV. SIMULATION RESULTS

Fig. 6: Interfacing With Processor

Fig. 7: Stage Control Reset Condition

Fig. 8: Input mux selection
V. CONCLUSION

An efficient method for stage control of launch vehicle is proposed here by the literature survey done on various papers. This method is based on processor (VIKRAM 1601) based system. This configuration enhances the system performance specially processing speed and computational margin with the available resources. Along with the control unit 32-bit pipelined processor has been developed and it has been used for executing navigation tasks on a prototyping board delivering outputs of desired accuracy. Here micro programming method is adopted to meet future requirement and it will be beneficial for future missile applications. Currently the computational margin available in 20 ms periodicity for satellite launch vehicles is the order of 3-4 ms which may increase to 8-9 ms with the processor scheme.

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