Adiabatic Logic Circuits for Low Power, High Speed Applications

Satyendra Kumar
M. Tech. Student
Department of Electronics & Communication Engineering
Shambhunath Institute of Engineering and Technology,
Jhalwa, Allahabad, Uttar Pradesh, India

Ram Raksha Tripathi
Assistant Professor
Department of Electronics & Communication Engineering
Shambhunath Institute of Engineering and Technology,
Jhalwa, Allahabad, Uttar Pradesh, India

Abstract

As technology is shrinking down we requires devices which consume less power gives less delay in device. So here we compare PFAL (Positive Feedback Adiabatic Logic) and ECRl (Efficient Charge – Recovery Logic) technique basic logic gates with CMOS gates. Results gives improvement in power and delay. Using this ECRL and PFAL we have design 2:1 mux which is very less power consuming and fast in operation. Simulation result is done using TSMC180nm technology on tanner tool.
Keywords: PFAL, VLSI, CMOS Logic, Adiabatic Logic, MUX, Adder

I. INTRODUCTION

Since the last few decades, the electronics industry has been growing enormously due to integrated circuit technology. Now, we have come a long way from the single transistor era of 1958 to ULSI (Ultra Large Scale Integration) which support the fabrication of more than fifty million transistors over a single chip. The increased use of portable electronics devices has made power dissipation an important design parameter in modern electronics. Portable devices that work using a battery have limited energy supplies and thus have a lifespan that are constrained by their power consumption. Until now, power consumption was not the greatest concern because of the availability of large packages and cooling techniques that have the capability of dissipating the generated heat. However, due to continuously increasing density as well as the size of the chips in the system might cause difficulty in providing adequate cooling and hence, add significant cost to the system. That is why we need a circuitry which can reduce power dissipation even if a number of components are integrated over a single chip. Our objective is to reduce the power dissipation in digital CMOS VLSI circuits.

The demand, of CMOS technology can be mainly attributed to lower power dissipation and high levels of integration. However, the latest trend towards ultra-low power has made researchers search for techniques to recover or recycle energy from the circuit. In recent days, researchers largely focused to find the lower bound of energy consumption. Different methods are commonly used for reduction of power dissipation in digital circuits, but most of the energy gets dissipated so, an adiabatic approach is the solution for the design of power and energy efficient designs. The amount of energy, recycle depends on fabrication technology, switching events, and the voltage swing.

This paper has been segmented into five sections. Section II describes a brief introduction about adiabatic logic. Section III focuses on logic design and operation. Section IV includes circuit implementation of digital circuits. Simulation waveforms and power comparison table explanation is in section V. and section VI focuses on conclusion.

II. ADIABATIC LOGIC

The term "Adiabatic" has been taken by thermodynamic means no energy transfer to the environment, so there is no dissipated energy loss. In real-life computing, because of the presence of dissipative elements like resistance in a circuit ideal process cannot be achieved. However, low energy dissipation can be achieved by slowing down the speed of operation and only switching transistor under certain conditions. Adiabatic circuits are low power circuits which need 'reversible logic' to conserve energy.

III. OPERATION OF ADIABATIC LOGIC

Adiabatic offers a way to reuse the energy stored in the load capacitor, rather than discharging the load capacitor to the ground and wasting this energy. Operations of adiabatic logic circuits are based on some basic rules such as never turn on a transistor when there is a voltage potential between the sources and drain terminals, and never suddenly change the voltage across any of the transistor.

IV. LOGIC DESIGN AND OPERATION

Positive Feedback Adiabatic Logic (PFAL) PFAL so called partial energy recovery circuit as it has a good robustness against technological variations. It is a dual rail circuit. The general schematic of PFAL is as shown in the figure below.

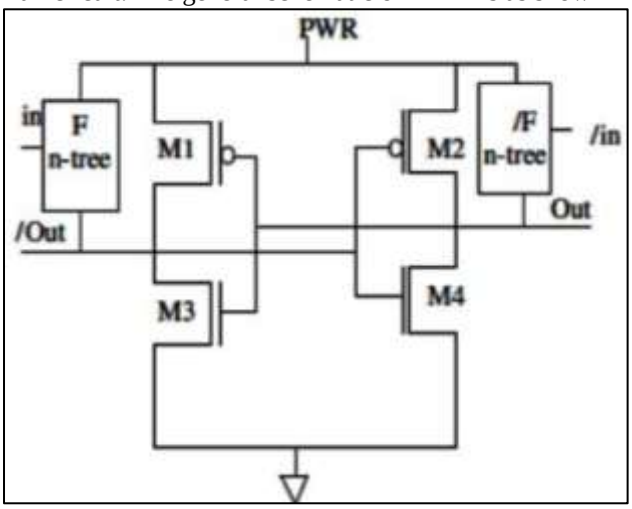

Fig. 1: Basic PFAL Structure

PFAL consist of a latch formed by two cross-coupled inverters to store the output state when input signal are ramped down. The two n-trees connected in parallel of PMOS realize the logic functions. The PMOSFET of the adiabatic amplifier is in parallel to the functional block and form a transmission gate. It uses four phase clock.

Efficient Charge – Recovery Logic (ECRL)

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong, shown in Figure 5, uses cross-coupled PMOS

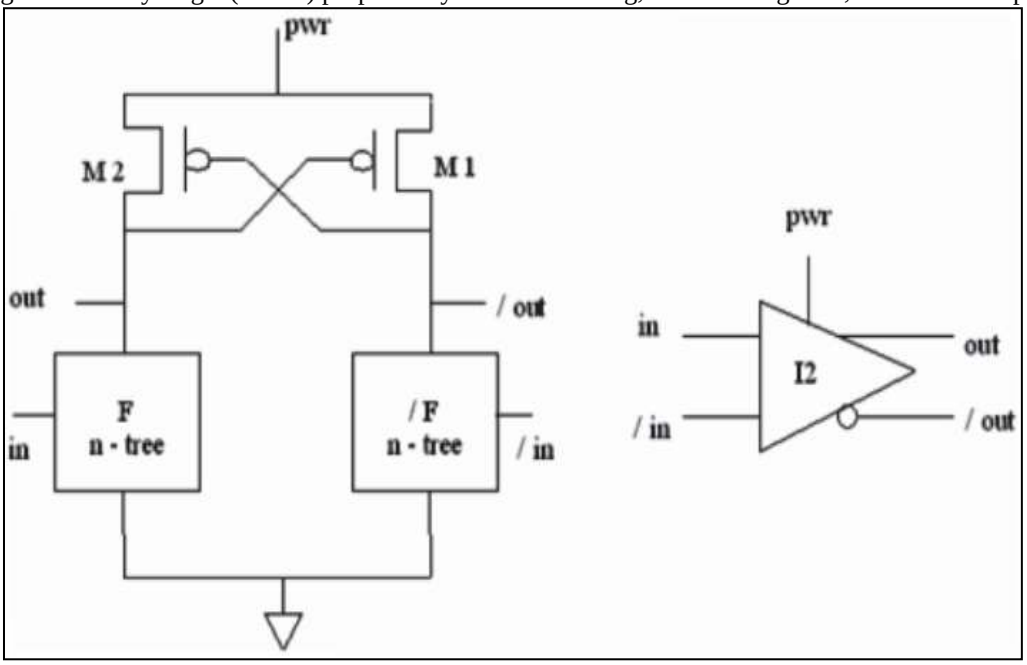

Fig. 2: Efficient Charge – Recovery Logic (ECRL)

It has the structure similar to Cascade Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block . An AC power supply *pwr* is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in. Full output swing is obtained because of the cross-coupled PMOS transistors in both pre charge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the pre charge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to |Vtp|, the PMOS transistor gets turned off.

V. CIRCUIT IMPLEMENTATION

A. Using PFAL

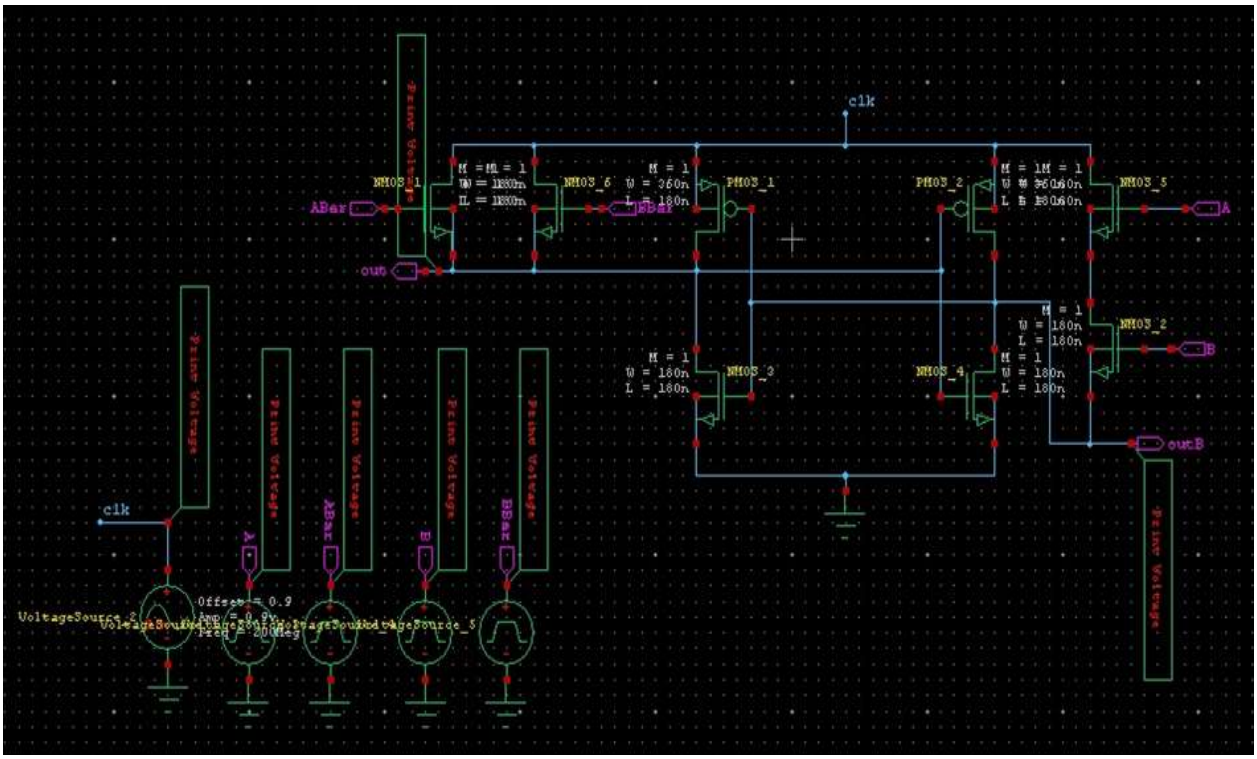

Fig. 3: PFAL NAND

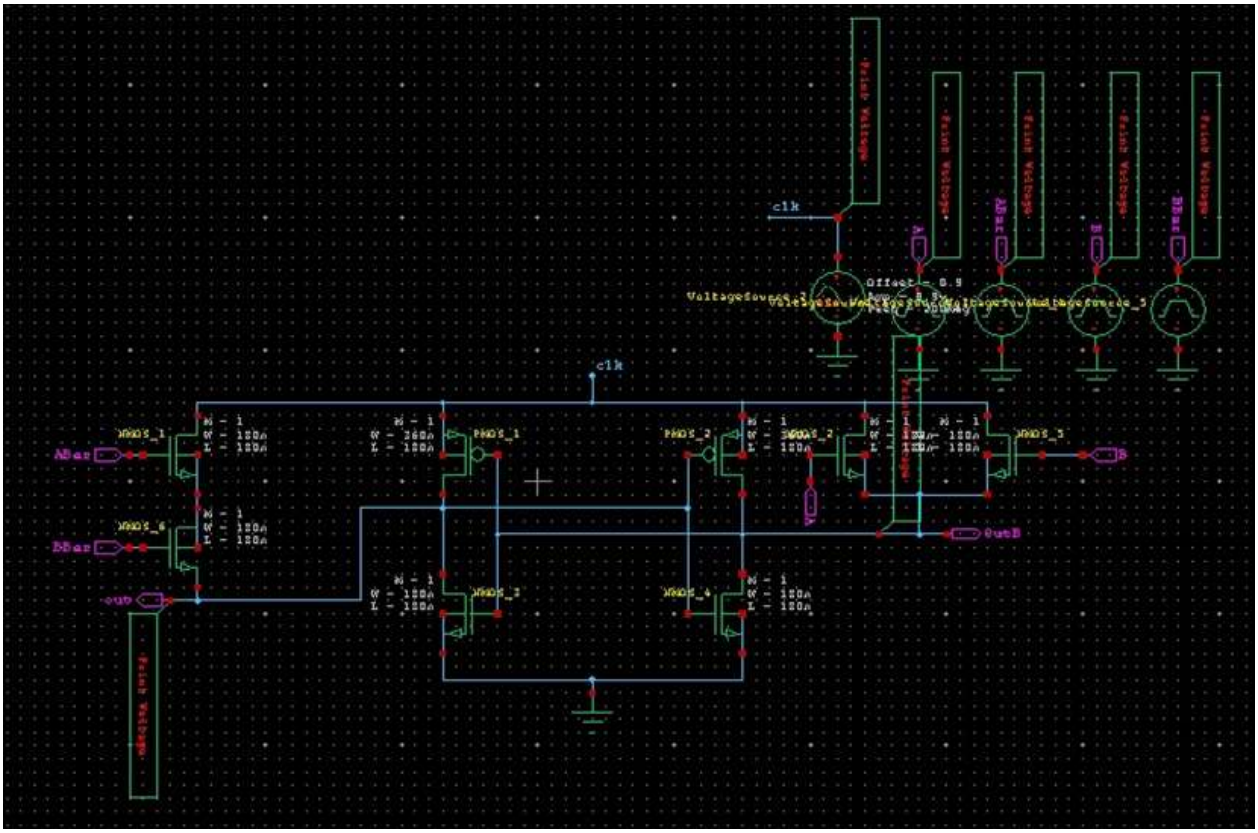

Fig. 4: PFAL NOR

B. Using ECRL

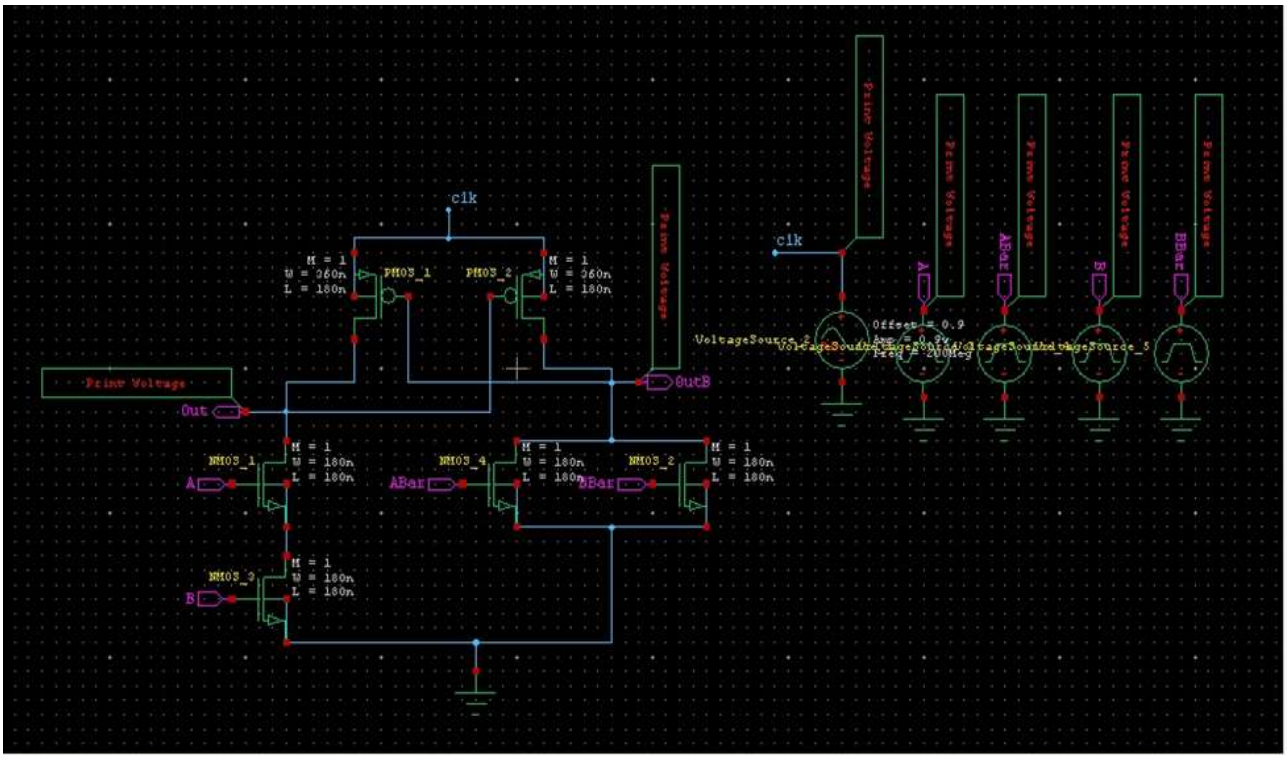

Fig. 5: ECRL NAND

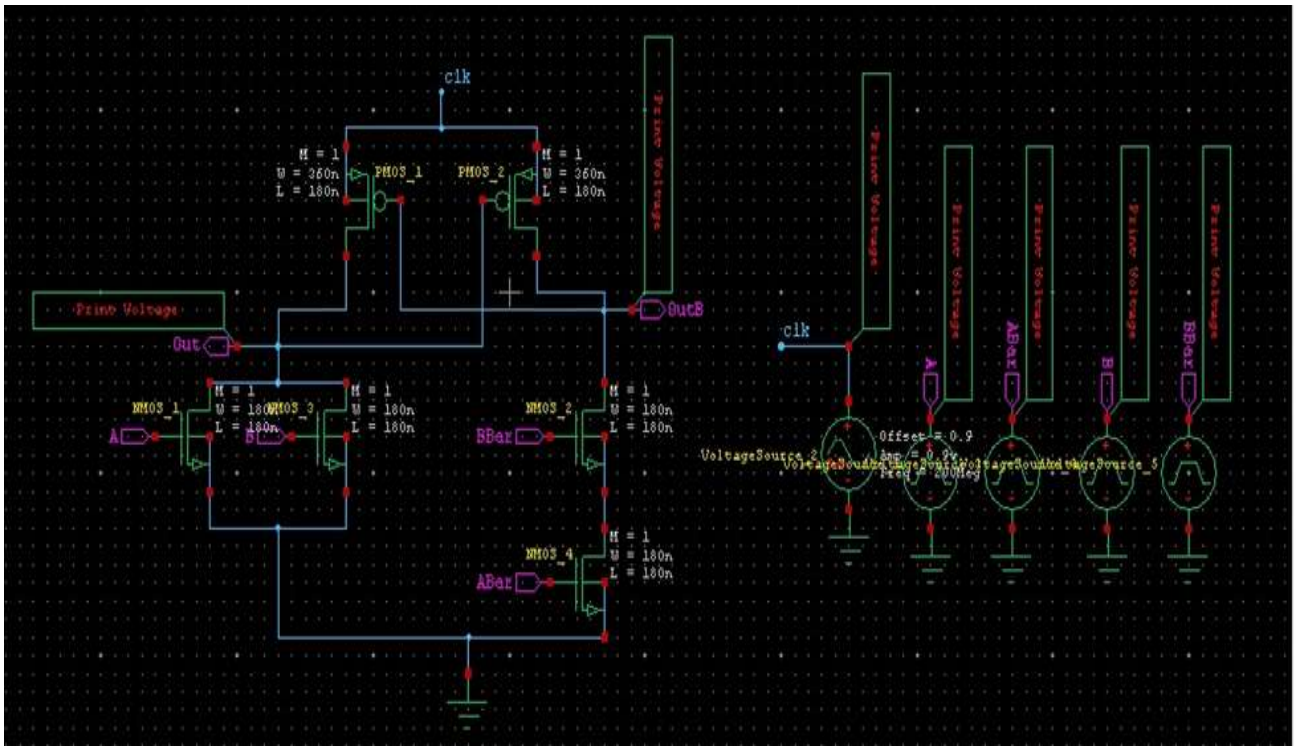

Fig. 6: ECRL NOR

VI. SIMULATION RESULT

In this paper, all the design structures based on conventional CMOS logic and adiabatic logic are designed and simulated on cadence virtuoso using 180nm technology. The comparison is performed using different frequencies and supply voltages. Power of CMOS and PFAL circuits is calculated for different frequency and supply voltage. And the effect of frequency on energy consumption is examined and compared with the result of conventional CMOS. Transient analysis results are as shown below.

Table - 1
CMOS Results

Parameter	*CMOS Inv*	*CMOS NOR*	*CMOS NAND*
Power (nw)	*3785*	*170*	*162*
Delay (ps)	*46829*	*19.5*	*26.4*
PDP (aj)	*17727*	*3.34*	*4.72*
Energy (fj)	*22713*	*27.3*	*28.3*

Table - 2
PFAL Results

Parameter	*PFAL Inv*	*PFAL Nor*	*PFAL Nand*
Power (nw)	*0.68*	*105*	*70.7*
Delay (ps)	*8.88*	*12.7*	*2.90*
PDP (aj)	*0.05*	*1.34*	*0.25*
Energy (fj)	*38.9*	*16.8*	*11.3*

Table - 3
ECRL Results

Parameter	*ECRL Inv*	*ECRL Nor*	*ECRL Nand*
Power (nw)	*0.30*	*50.9*	*26.2*
Delay (ps)	*26.1*	*82.7*	*49.4*
PDP (aj)	*0.07*	*4.21*	*1.29*
Energy (fj)	*18.2*	*8.1*	*4.19*

A. PFAL

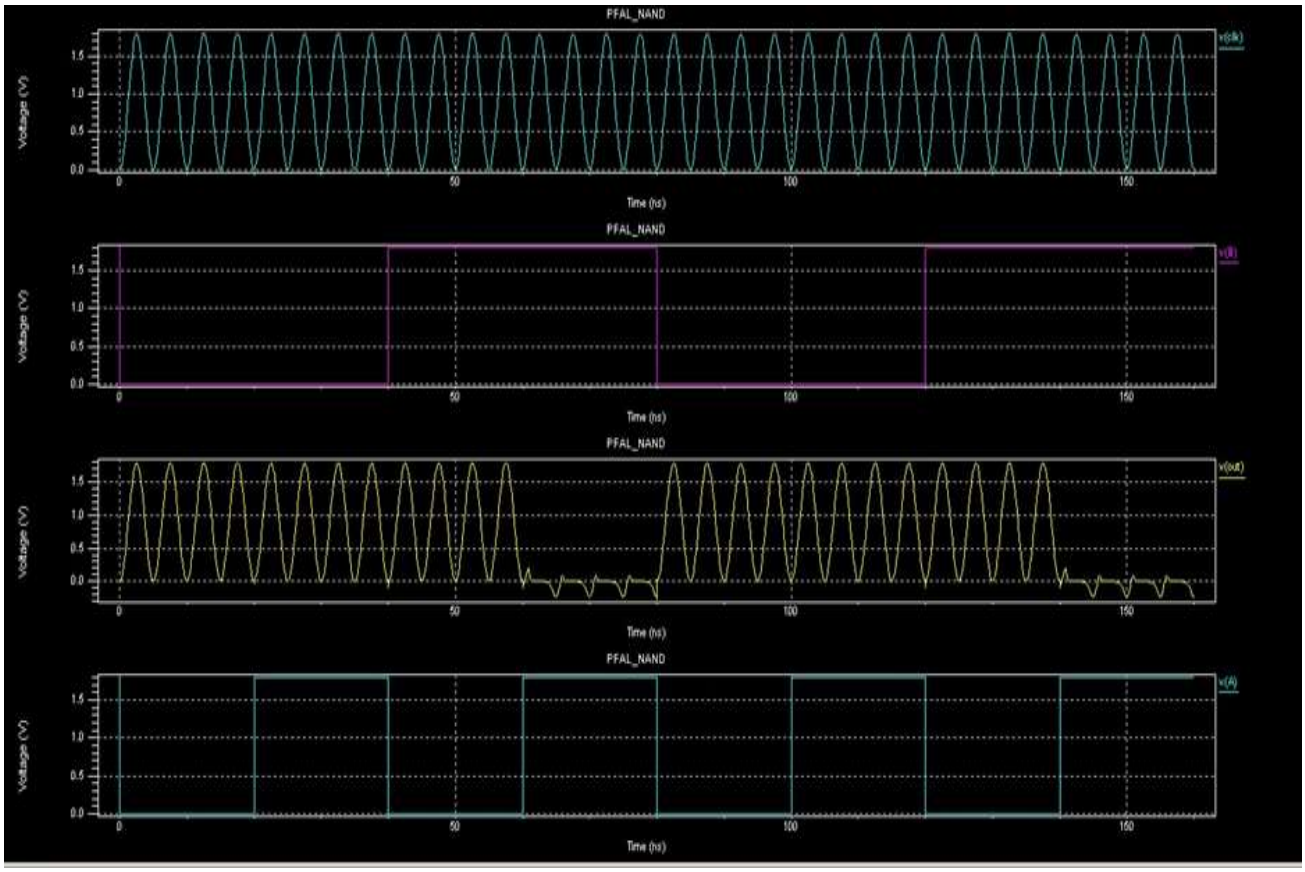

Fig. 7: PFAL NAND waveform

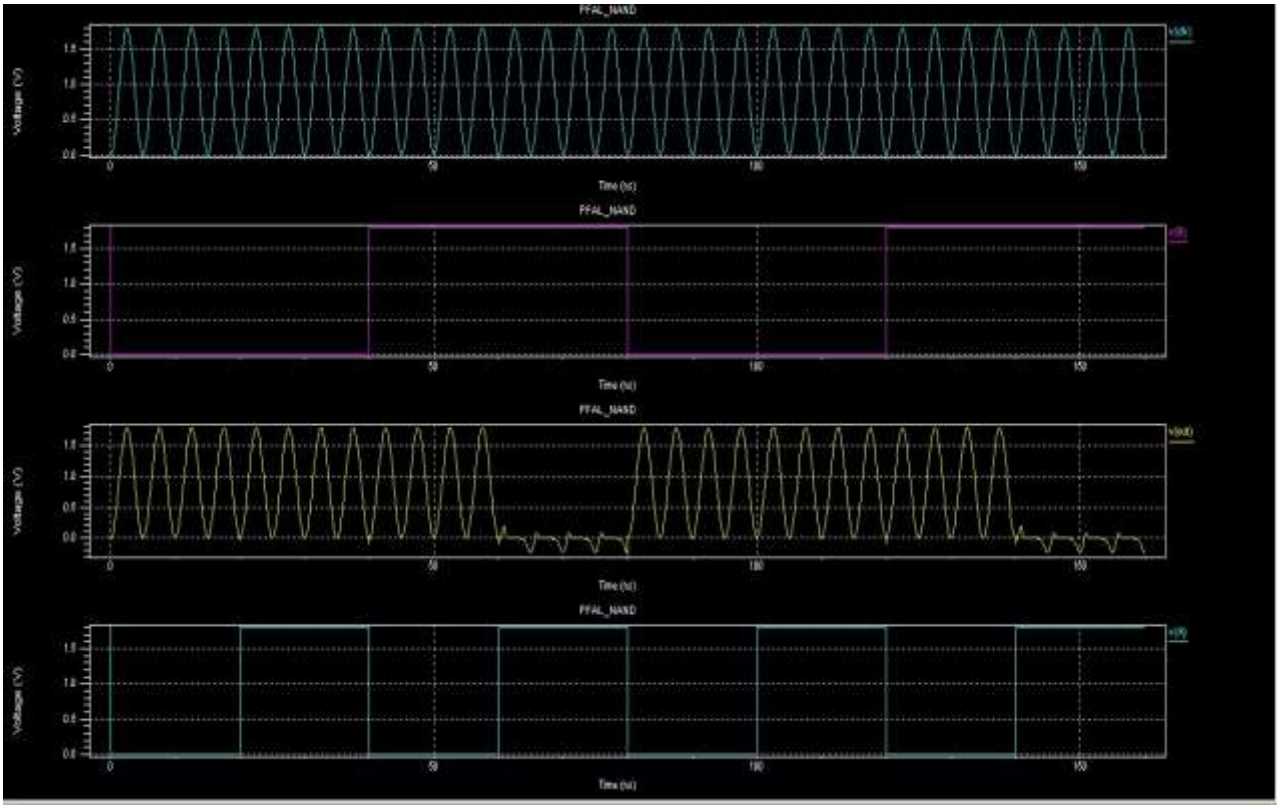

Fig. 8: PFAL NOR waveform

B. ECRL

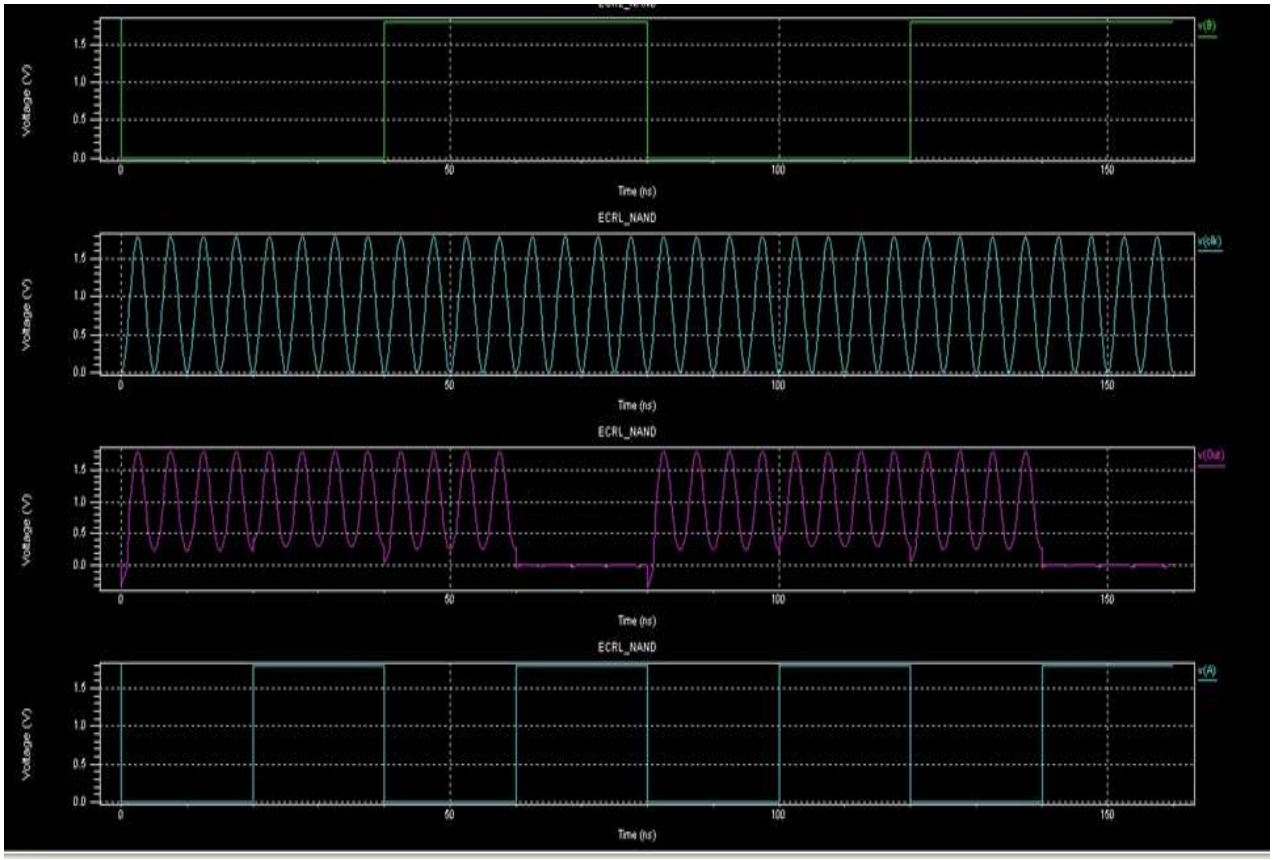

Fig. 9: ECRL NAND waveform

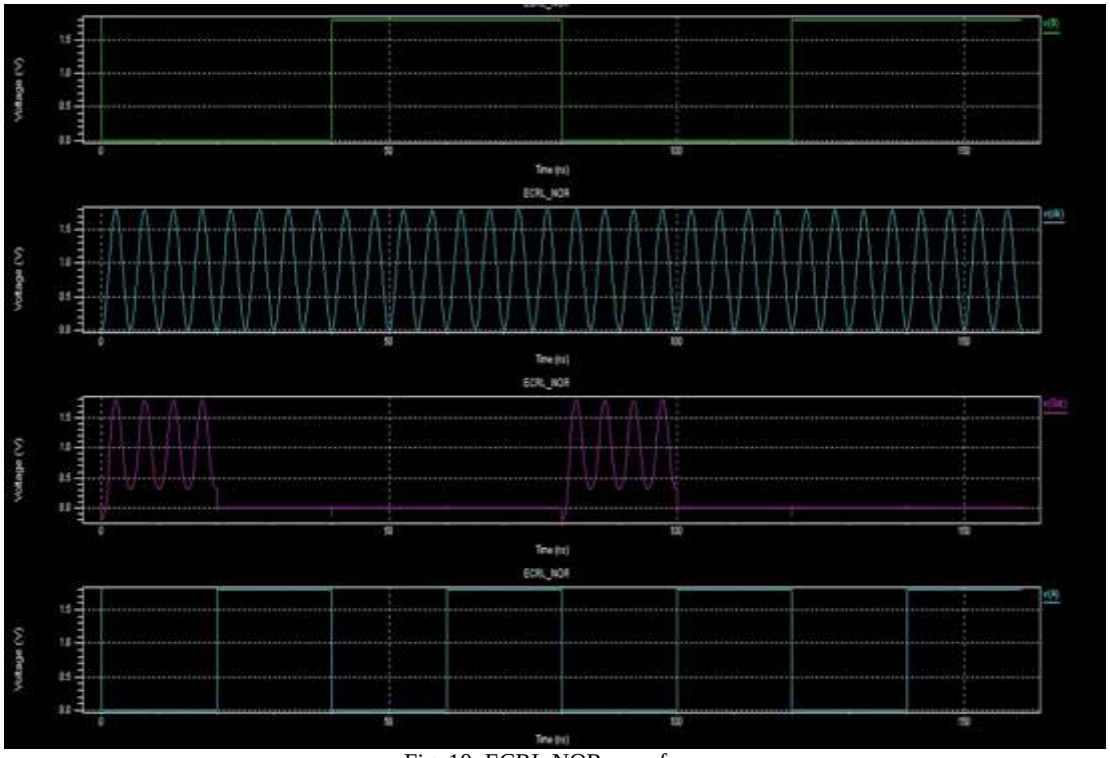

Fig. 10: ECRL NOR waveform

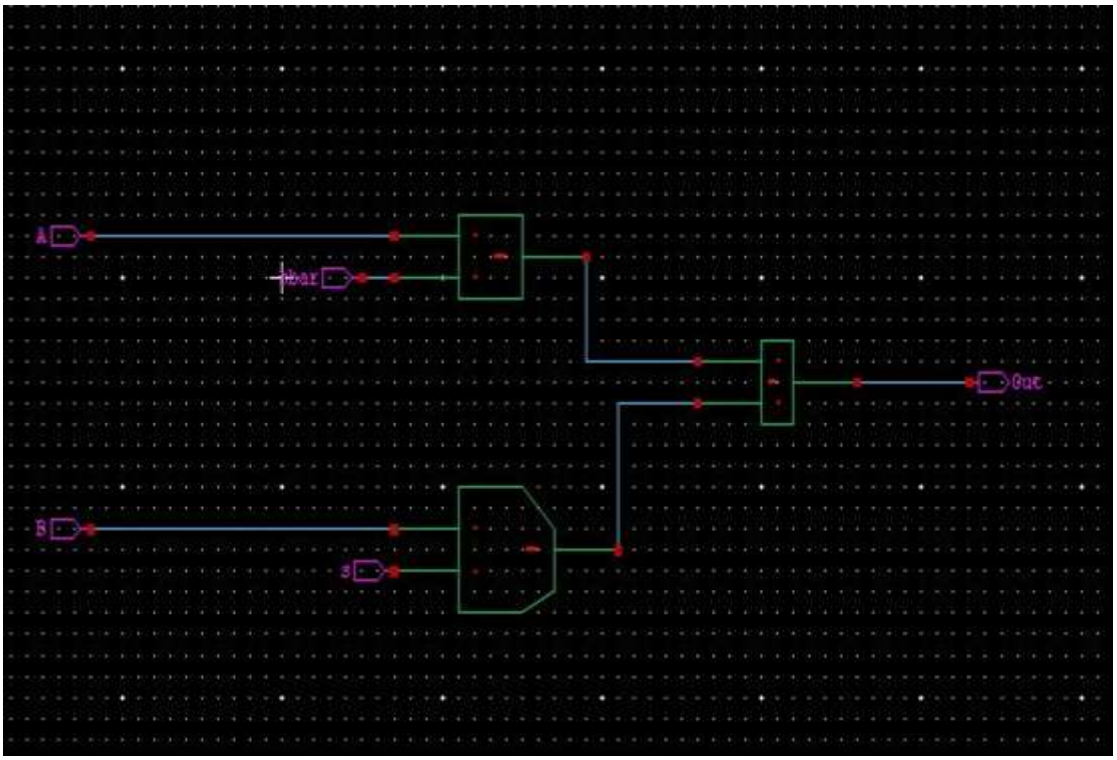

Fig. 11: 2:1Mux

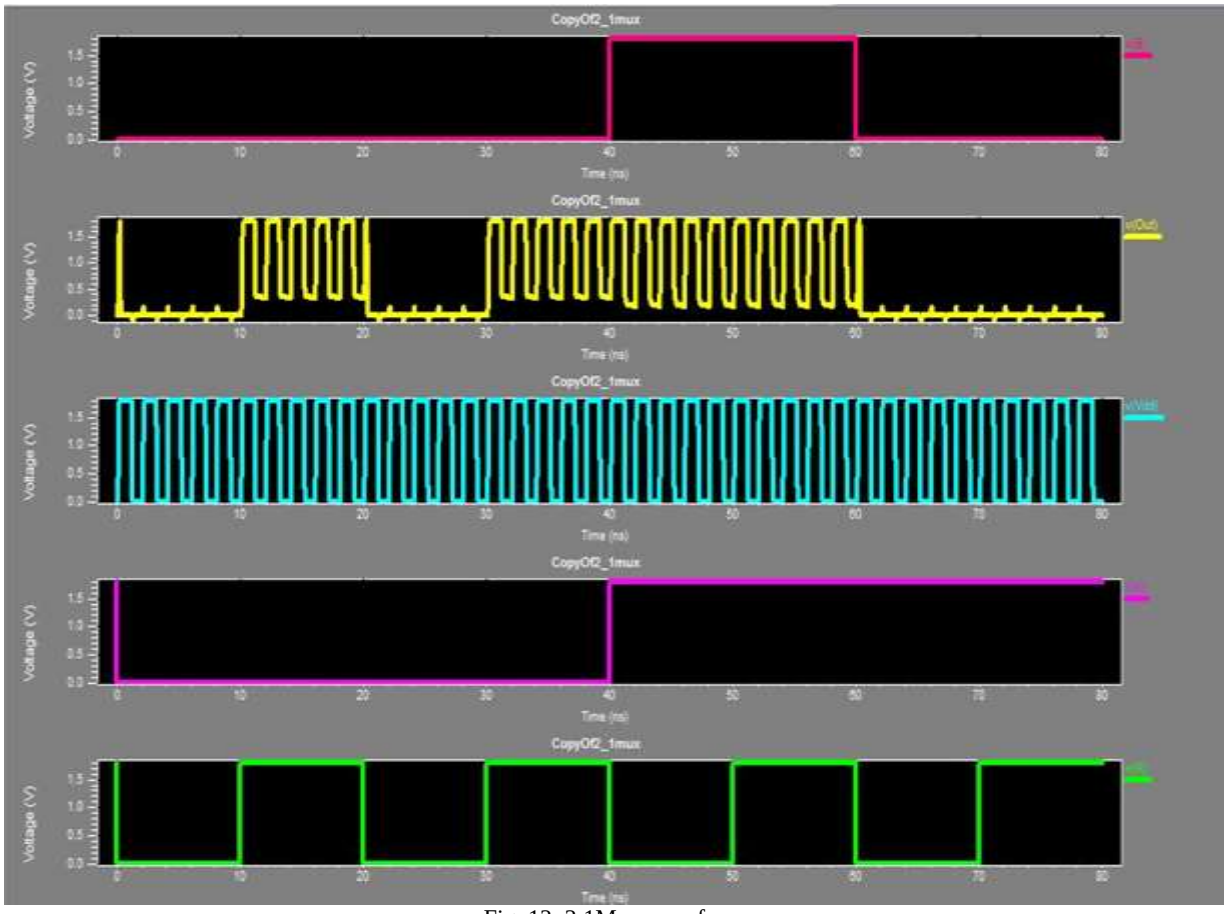

Fig. 12: 2:1Mux waveform

VII. CONCLUSION

After comparing results of PFAL and ECRL basic gates with CMOS gates we got good improvement in results. As industry demands devices with low power and fast operating ECRL and PFAL logic gates are most suitable and useful in any circuitry. This basic gates ca be used in building adder, full adder, multiplexer, flip-flop. Here we have made 2:1 mux using PFAL and ECRL gate which is very fast in operation and less power consuming.

REFERENCES

[1] W. C. Athas, L.J. Svensson, J.G. Koller, N. Tzartzanis, and E. Chou,"Low power digital systems based on adiabatic-switching principles,"IEEE Trans. VLSI Systems, vol. 2, no. 4, pp. 398-407, Dec. 1994.
[2] J. S. Denker, "A review of adiabatic computing," in IEEE Symp. On Low Power Electronics, pp. 94-97, 1994.
[3] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design,'' IEEE J. Solid-State Circ., vol. 27, no. 4, pp. 473-484, Apr. 1992.
[4] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," IEEE J.Solid-State Circuits, vol. 30, pp. 311–315, Mar. 1995.
[5] J. G. Koller and W. C. Athas, "Adiabatic switching, low energy computing, and the physics of storing and erasing information," IEEE Press, in Pmc. Workshop on Physics and Computation, Phys Cmp '92.oct. 1992.
[6] T. Gabara, "Pulsed Power Supply CMOS," Technical Digest IEEE Symposium Low Power Electronics, San Diego, pp. 98- 99, Oct. 1994.