Design and Implementation of Testable Reversible Universal Shift Register

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Abstract

The design of testable universal shift register based on conservative logic is tested for unidirectional stuck-at faults by using two test vectors i.e. all 1’s and 0’s. The important memory element in family of sequential circuits is Universal Shift Register. In this project design of sequential application circuits like Universal Shift Register is done by using reversible gates such as Fredkin, Feynman and Peres gates. The proposed 4*4 reversible universal shift register can identify single missing line stuck at faults in the circuits and also it reduces the quantum cost, delay and garbage outputs as well as testability. The important memory element in family of sequential circuits is Universal Shift Register. In this project design of sequential application circuits like Universal Shift Register is done by using reversible gates such as Fredkin, Feynman and Peres gates. The design of testable universal shift register based on conservative logic is tested for unidirectional stuck-at faults by using two test vectors i.e. all 1’s and 0’s. The proposed 4*4 reversible universal shift register can identify single missing line stuck at faults in the circuits and also it reduces the quantum cost, delay and garbage outputs as well as testability.

Keywords: Flip-Flop, Multiplexer, Reversible Logic, Reversible Gate, Shift Register, Quantum Cost, Garbage Output

I. INTRODUCTION

In now day’s reversible logic has been considered as an essential concern for computer design. Revisable gates increasing application of low power devices. Shift Register consists of group of flip flops connected corresponding the information bits can be shifted right are left depending on the selection line. Reversible circuits are of great absorption in the range of low power CMOS design, quantum computing, optical computing and nano-technology. Conservative logic is a logic family that performance the effects that there are an equal number of 1s in the outputs as there are in the inputs. Irreversible computation 1 bit of information lost and fans out problem will affected by conventional gates; result by KTln2 joules of energy dissipation, the K is the Boltzmann’s constant T is the absolute temperature.

Conservative logic sometimes revisable and sometimes used the not be reversible in nature. Zero internal power dissipation advantage to the conservative logic proposed technique. The conservative logic line approach offered by avoids number dead ends, and fan out problem is not allowed in this technique.

A. Basic of Revisable Gates:

- Fredkin gate (CSWAP)
- Feynman gate (CNOT)
- Peres gate
- Toffoli gate
- Not gate
- Double Feynman gate

Different 3 vectors reversible logic gates like as Peres gate, Toffoli gate, Fredkin gate and 2 vector logic such as Feynman gate have been literature. Reversible gates quantum cost defined as the primitive gates. Quantum cost design defined on the vector like 1x1, 2x2, 3x3 reversible gates. 1x1, 2x2 reversible gates are considered as unity so quantum cost is one. Realize using not gate vector 1x1 and 2x2 reversible gates such as controlledV, controlledV+, V is the square root of NOT gate, V+ is hermitian. The Feynman gate is all controlled NOT (CNOT). Quantum cost can be calculated using controlledV, controlledV+ and CNOT gates can be implemented using the above condition.
B. Conservative Logic Based Fredkin Gate:

![Fredkin Gate Diagram](image)

Fig. 1: fredkin gate

Fig 1 shows Fredkin gate is a 3x3 gate and universal gate 3 input and 3 output any logical or arithmetic operation done by fredkin gate. The input vector I(A,B,C) & output vector (P,Q,R). the output vector defined (P=\(A\), Q=\(A'B^AC\), And R=\(A'C^AB\)). The quantum cost of fredkin gate is 5.

C. Related Work:

The design of revisable universal shift register circuits is addressed in the alternatives interesting augmentation in which designs are enhanced terms of different functions, a like as the number of revisable gates, garbage outputs, quantum cost, delay and testing complexity etc. To the best of our understanding offline testing of revisable universal shift register to shift right are left depending on the design. In this, paper design of Revisable universal shift register that can be tested for two test vectors, all 0’s and all 1’s for any single line missing stuck at faults. By giving both test vectors 0 we test for stuck-at-1 fault and similarly if give the both test vector input are 1 means we test for stuck-at-0 fault.

II. DESIGN OF TESTABLE REVERSIBLE LATHES AND MULTIPLEXER

A. Design of D Latch:

The D latch characteristic equation written as the \(Q+=D\cdot E+E'\cdot Q\), D is the input of flip flop and E is the enable and Q is the inout of the flip flop. in the proposed work enable refers to the clock and enable equal in value place of clock. when the enable signal is high the value of the latch output is reflected at the input of D latch the output is \(Q+=D\). while enable is low the output of D latch is \(Q+=Q\).

![D Latch Diagram](image)

Fig. 2: Reversible D latch

B. Design of Testable Reversible D Latch:

Our proposed work of the two fredkin gate cascade connection the output of first fredkin gate Q while follow the other and two control signals such as C1 and C2 design the second fredkin gate remaining two inputs and output of second fredkin gate Q and other one inout terminal and 3rd one garbage output.

![Testable Reversible D Latch Diagram](image)

Fig. 3: Design of testable reversible D latch using fredkin gate
C. Design of 4:1 Multiplexer:

The Multiplexer two control signal S0 and S1 used to perform left and right shift and parallel transfer the input data. The multiplexer selected line S1S0=00 present value of the input and select line S1S0=01 shift left, and S1S0=10 shift right operation and S1S0=11 Parallel loading operation.

![4:1 multiplexer using fredkin gate](image)

Fig. 4: 4:1 multiplexer using fredkin gate

III. DESIGN OF REVERSIBLE UNIVERSAL SHIFT REGISTER

If the register is there shift that can shift the data in only one direction, either from left to right or from left they can call it unidirectional shift register. The register that can shift the data in both directions from left to right and right to left they call it bidirectional shift register. have the bidirectional shift register as well as the parallel loading then that shift register is called universal shift register. Parallel loading means the data stored in the flip flop input entered into the parallel manner or we can say simultaneously.

![4 bit Reversible universal shift register](image)

Fig. 5: 4 bit Reversible universal shift register

Table 1

<table>
<thead>
<tr>
<th>Mode control</th>
<th>Register operation</th>
</tr>
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<tbody>
<tr>
<td>S1 S0</td>
<td></td>
</tr>
<tr>
<td>0 0</td>
<td>No change</td>
</tr>
<tr>
<td>0 1</td>
<td>Shift Right</td>
</tr>
<tr>
<td>1 0</td>
<td>Shift left</td>
</tr>
<tr>
<td>1 1</td>
<td>Parallel load</td>
</tr>
</tbody>
</table>
The multiplexer two control signal S1 and S0, which is used to perform the operation of shift left, right parallel loading. the input value S1S0=00 No change the register operation the multiplexer selected input 0. The input value S1S0=01 multiplexer selected input 1 and thus the right shift operation take place. The input value S1S0=10 multiplexer selected input 2 and thus the left shift operation take place. When the select line S1S0=11 the multiplexer selected input 3 and thus the parallel load operation take place in universal shift register


<table>
<thead>
<tr>
<th>Design of reversible universal shift register</th>
<th>Quantum cost</th>
<th>Delay</th>
<th>Garbage output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed</td>
<td>110</td>
<td>110</td>
<td>34</td>
</tr>
<tr>
<td>Existing</td>
<td>144</td>
<td>144</td>
<td>35</td>
</tr>
<tr>
<td>Improvement (%) w.r.t[10]</td>
<td>23</td>
<td>23</td>
<td>1.4</td>
</tr>
<tr>
<td>Improvement (%) w.r.t[9]</td>
<td>8</td>
<td>8</td>
<td>11</td>
</tr>
</tbody>
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**IV. OUTPUTS**

Fig. 6: Simulation of D latch

Fig. 7: Simulation of testable reversible D latch in normal mode

In test mode stuck at-0 fault when C1C2=11 make the design of testable with all C1 and C2 are both are high input vectors as output T1 will becomes high resulting in making testable with all 1s in the input vector.
A universal shift register when the test vectors C1C2=01, the normal mode of shift register and select line is both are high then input will be 1010 the output will be parallel loading 1010.

A reversible universal shift register when the input test vectors all are zero the output of shift register all are low and select line is both are high but do not parallel load of the universal shift register because the stuck at-1 fault of the circuit as shown in fig 9.
A stuck at-0 fault reversible universal shift register, when the test vector C1C2=11 the output of the 4 bit universal shift register all are high and select line will be high but do not parallel loading because stuck at-0 fault of the circuit.

V. CONCLUSION

The proposed testable reversible universal shift register uses conservative logic method to test for any stuck at fault by using two test vectors named as 0s and 1s. In this method reversible flip flop circuits are employed for designing complex sequential circuits of universal shift register. The proposed method can be applied in the real-time application of fault coverage by a single missing/additional cell and in testing sequential circuits. The proposed method uses less number of reversible gates in order to reduce circuit complexity. This method in turn reduces the number garbage outputs 1.8%, quantum cost 22%, delay 22% and testability complexity.

VI. FUTURE SCOPE

1) This method further can be applied for combinational circuits such as datapath elements viz, adders, substractors, multipliers and encoder, decoder design and comparator design.
2) By increasing bit size in the universal shift register this method can be employed in designing counter circuits.
3) Further this method of testability can be applied for a complete Processor design using reversible logic components and using reversible instruction set.
4) This method can also be applied for Multi-Core Processor Design.

REFERENCES