Reduction of Power Dissipation in SRAM using Adiabatic Logic

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Abstract

Static RAM is a temporary storage memory used in cache memory. It is a fast access memory and it is prone to high power dissipation. Adiabatic logic technique is one among the many low power techniques in VLSI design to reduce power dissipation. Adiabatic logic is implemented to SRAM to reduce power dissipation. Among the various adiabatic techniques, Split Level Charge Recovery Logic (SCRL) is used to reduce power dissipation in SRAM. Adiabatic logic is implemented for conventional 5T SRAM in this paper. The operation of adiabatic logic implemented SRAM is similar to the operation of conventional SRAM. Clocks have been used instead of DC supply and transmission gates are used. Size of the SRAM becomes large but it is overcome by reduction in the power dissipation. Simulation is done in 45nm technology using Cadence.

Keywords: 5T SRAM, Adiabatic Logic, Cache Memory, SCRL, Transmission Gates

I. INTRODUCTION

SRAM is static memory which holds information cross coupled inverter until power is being applied to cross coupled inverter. It does not need periodic refreshing like DRAM and it is faster and expensive than DRAM and consumes less power than DRAM. To reduce the power dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, or he can minimize the voltage swing, or he can apply a combination of these methods. Adiabatic logic circuits offers the possibility of reducing energy dissipation during the switching events and the possibility of recycling, reusing some of the energy drawn from the supply. Adiabatic logic reuses the energy stored in the load capacitors instead of discharging the load capacitors to the ground like conventional way and wasting that energy.

II. CONVENTIONAL 5T SRAM

Fig 1 shows schematic conventional 5T SRAM. WL denotes Word Line, BL denotes Bit Line, D denotes data stored in SRAM cell and Dbar denotes complement of D. WL is made high to turn on the access transistor n1. DC supply voltage VDD is applied to cross coupled inverters. For storing 1, BL is made high and 1 is passed through access transistor to D node. The value at D serves as input to second inverter and this inverter outputs the complement value of D. The value at Dbar serves as input to first inverter. The output of first inverter will be the complement of value at Dbar. That output value will be the value which was passed through access transistor. Hence at any time, the value at D node will the value which was sent to store in SRAM through access transistor n1. The same operation holds good for storing 0 into the SRAM cell.

III. PROPOSED 5T SRAM

Fig 2 shows circuit of adiabatic 5T SRAM. Clock supply is used for inverters instead of DC supply. The charging and discharging of gate capacitor is slowed down by using a clock with suitable rise and fall times. Hence the time period T, which is charging period, increases. As per the energy dissipation formula \( E_{Diss} = C V_{DD}^2 \frac{RC}{T} \), if charging time increases, energy dissipation decreases. Fig 3 shows the trapezoidal clocks used in the proposed 5T SRAM cell.
Initially nodes n1 and n2 are at V_{DD}/2. Potential difference across transistors are maintained at V_{DD}/2 using transmission gates. Φ1, Φ1bar, Φ3, Φ3bar are initially at V_{DD}/2. Φ2 and Φ4 are initially at 0 V and Φ2bar and Φ4bar are initially at V_{DD} making the transmission gate off. To store the value in the cell, the access transistors are made on by making word line voltage high. Then the value is applied to the bit line. The access transistors passes the value to the D node. The value at the D node will act as input to the first inverter.

The voltage at Φ1 changes from V_{DD}/2 to V_{DD} and the voltage at Φ1bar changes from V_{DD}/2 to 0. The inverter becomes on and complement of data bit at D node will be the output of the inverter. Φ1 and Φ1bar changes to V_{DD}/2.

Then Φ2 changes from 0 to V_{DD} and Φ2bar changes from V_{DD} to 0 and the transmission gate becomes on. The output of the inverter is fed to input of another inverter through the transmission gate. Φ2 becomes 0 V and Φ2bar becomes V_{DD} and the transmission gate becomes off.

The clock Φ3 changes from V_{DD}/2 to V_{DD} and Φ3bar changes from V_{DD}/2 to 0. The inverter becomes on and the complement of the value at Dbar node becomes output of the inverter. Again Φ3 and Φ3bar becomes V_{DD}/2.

Then Φ4 changes from 0 to V_{DD} and Φ4bar changes from V_{DD} to 0 and the transmission gate becomes on. The output of the inverter is fed to input of another inverter through the transmission gate. Φ2 becomes 0 V and Φ2bar becomes V_{DD} and the transmission gate becomes off.

This cycle repeats until new value is written to the cell. The output waveforms is shown in fig 4 and layout of adiabatic 5T SRAM is shown in fig 5.

![Proposed 5T SRAM](image1)

![Trapezoidal clocks for proposed 5T SRAM](image2)

![Output waveform](image3)

![5T Adiabatic SRAM layout](image4)

**IV. CONCLUSION**

Adiabatic logic implemented to conventional 5T SRAM reduced the power dissipated from it. Efficient energy recycling is done by using trapezoidal clocks. Minimum potential difference is maintained across the transistors of the cell using transmission gates. Split level charge recovery logic (SCRL) is used for reducing power dissipation of SRAM. Conventional 5T SRAM and adiabatic 5T SRAM are simulated using cadence virtuoso 45nm technology. Conventional 5T SRAM has dissipated 122.2 nW of power. Proposed adiabatic 5T SRAM has dissipated 10.68 nW of power thereby reducing power dissipation by a considerable amount.

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