Multilevel Power Optimization for ICA Processor

Jini Kuriakose
Assistant Professor
Department of Electronics & Communication Engineering
MA College of Engineering, Kothamangalam

Jayan K George
Assistant Professor
Department of Electronics & Communication Engineering
MA College of Engineering, Kothamangalam

Abstract

This paper presents a 16-channel ICA implementation in FPGA for biomedical application. Independent component analysis (ICA) is a statistical signal processing technique having emerging new practical applications. Infomax ICA is a common method to identify artifacts and interference from their mixtures such as electroencephalogram (EEG), magnetoencephalography (MEG), and electrocardiogram (EEG). Multilevel power optimization approach is used for reducing the power dissipation of the ICA processor.

Keywords: Independent component analysis (ICA), Infomax, Multilevel Power optimization

I. INTRODUCTION

The EEG recorded from the scalp provides important information about the health of the central nervous system [1]. The measured EEG is often contaminated by artifacts and electric noise. This problem can be solved by the independent component analysis (ICA) algorithm [2]. The main bottleneck of multi-channel ICA is the computation complexity and hardware cost. The purpose of this study is to propose 16-channel ICA architecture with real time separation of EEG signals.

ICA recovers independent source signals from their mixed signals by finding a linear transformation that maximizes the mutual independence of mixtures. To improve the efficiency of ICA, Extended Infomax algorithm is proposed. Infomax ICA measures non-Gaussianity using kurtosis to find the independent sources from their mixtures [3]. However, most of the publications focused on offline signal processing using FastICA algorithm. It cannot be applied to real-time applications such as speech signal enhancement [4] and EEG/MEG essential features extraction for brain computer interface (BCI) [5]. In order to realize the real-time signal processing, the FastICA algorithm can be implemented on a field-programmable gate array (FPGA) to speed up the computation involving vector multiplications, matrix multiplications, and matrix inverses.

For portable and long-term monitoring applications, the power consumption is an important design trade-off consideration [6]. One of the most critical design requirements for portable biomedical devices is the capability to operate with minimal energy, in order to maximize battery operating time. This paper focuses on the multilevel power optimization for ICA processor.

In this paper a low power ICA processor is proposed. In order to minimize the power consumption, the multilevel power optimization methodology is used. The rest of the paper is organized as follows: section II briefly introduces the short description of the independent component analysis theory. Simulation result is provided in section III and finally a conclusion is given in section IV.

II. INDEPENDENT COMPONENT ANALYSIS

Independent component analysis (ICA) [7] is a well-known method of finding latent structure in data. ICA is a statistical method that expresses a set of multidimensional observations as a combination of unknown latent variables. These underlying latent variables are called sources or independent components and they are assumed to be statistically independent of each other. The ICA model is

\[ x = f(\theta, s) \] (1)

where \( x = (x_1, \ldots, x_m) \) is an observed vector and \( f \) is a general unknown function with parameters \( \theta \) that operates on statistically independent latent variables listed in the vector \( s = (s_1, \ldots, s_n) \). A special case of (2.1) is obtained when the function is linear, and we can write

\[ x = As \] (2)

where \( A \) is an unknown \( m \times n \) mixing matrix. In Formulae (1) and (2) we consider \( x \) and \( s \) as random vectors. When a sample of observations \( X = (x_1, \ldots, x_N) \) becomes available, we write \( X = AS \) where the matrix \( X \) has observations \( x \) as its columns and similarly the matrix \( S \) has latent variable vectors \( s \) as its columns. The mixing matrix \( A \) is constant for all observations.

If both the original sources \( S \) and the way the sources were mixed are all unknown, and only mixed signals or mixtures \( X \) can be measured and observed, then the estimation of \( A \) and \( S \) is known as blind source separation (BSS) problem.

The linear model (2) is identifiable under the following fundamental restrictions: the sources (i.e. the components of \( S \)) are statistically independent, at most one of the independent components \( s_j \) may be Gaussian, and the mixing matrix \( A \) must be of full column rank. The identifiability of the model is proved in the case \( n = m \) and for those source densities whose variance is defined.
ICA Definition: “Independent Component Analysis (ICA) is a method for finding underlying factors or components from multivariate (multi-dimensional) statistical data. What distinguishes ICA from other methods is that it looks for components that are both statistically independent and non-Gaussian.”

III. SYSTEM OVERVIEW AND ARCHITECTURE

FPGA technology is very suitable to implement the digital signal processing algorithm for quickly verifying the algorithm in hardware. For real-time implementation of the FastICA algorithm, it requires high volume of mathematical operations in a very short time interval. Currently, most FPGAs have on-chip hardware multipliers and memory blocks, and are suitable for such application. In this paper, the hardware ICA is implemented by hand coding VHDL hardware description language (VHDL). To increase the feasibility in the implementation of higher dimensions of ICA, the design of implementation of ICA is based on the concept of modules.

The block diagram of the pipelined ICA with its peripherals is illustrated in Fig.2. It includes five module boards: 1) mixed signals amplifier and filter module; 2) ADC circuit module; 3) FPGA chip containing pipelined ICA algorithm hardware; 4) DAC circuit module; and 5) the signal output processing module of estimated independent component signal. Each module board has dual channel signal processing capability. Both ADC and DAC have 24–bit resolution. Moreover, ADC and DAC chips select 8-pin dual in-line package (DIP) with serial control interface to reduce the FPGA’s input/output (I/O) ports expense.

The ICA engine is a chip implementation of the Infomax ICA [8] algorithm as shown in Fig.1. The EEG sample input buffering and calculation unit implementing the data windowing and operation schedule scheme. An ICA computation unit for unmixing the independent source signals from the multichannel EEG input. An ICA training unit for calculating the unmixing weight matrix for use in the ICA computation unit. A preprocessing whitening unit for reducing the number of training iterations and accelerating convergence in the ICA training unit. Reduction in computation complexity and chip power consumption are achieved through the introduction of the whitening operation at the algorithm level.

With ongoing trend of increasing integration synthesized digital circuit and custom analog circuit, power dissipation from both types of circuit blocks must be considered in order to achieve an overall low power dissipation of VLSI systems [9]. The focus of this paper is to demonstrate a design approach that minimizes power dissipation of analog mixed-signal building blocks. Multilevel power optimization technique is used for the minimizes the power dissipation. Pipelined analog to digital converter, a popular ADC architecture [10] for medium to high resolutions, is one such building block that are commonly used in modern mixed signal ICs. To minimize the power dissipation, a number of approaches have been proposed from a wide range of perspectives. At the circuit level, device types and supply voltages are jointly optimized for the residue amplifier of a pipeline stage to minimize power. At the architecture level, a non-linearity contribution from stage gain error is optimally distributed to further minimize combined power dissipation.

The proposed pipelined ICA focuses on 16 channels in this paper. It had been verified. A n–dimensional ICA architecture based on the proposed hardware modules is illustrated in Fig.3. The size of the submemory is 32 by m , where is the number of time samples.

IV. SIMULATION RESULTS

A VLSI architecture for 16-channel real time ICA was presented. Test signals are fed to the chip through a Xilinx FPGA verification suite and channel outputs are matched against MATLAB ICA simulation.
Fig. 2: Block diagram of pipelined ICA

Fig. 3: The n-dimensional ICA architecture

V. CONCLUSION

VLSI implementation of ICA algorithm offers many features such as high processing speed, which is extremely desired in many applications. In order to reduce the complexity, the Fast ICA block is divided into several sub modules and each of the sub modules are developed by HDL coding.
REFERENCES


