Implementation of Full Adder using Single Electron Transistor, SET: The Next Generation Nano Device

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Abstract

For the next generation VLSI circuits with high density, the most efficient device that can be used in basic circuits is the Single electron devices because they consume very low power and the package density. Single electron transistor [SET] is a new evolution in nanotechnology. It can be scaled to a great extent almost to that of atomic scale. It has unique characteristics of controlling one electron at a time. In an SET the number of electrons involved in logic operations is very less. Hence, the power consumption also minimizes to a great extent. As the electrons are quantized, the operating speed is very high and finds its application in many VLSI circuits. This paper presents implementation of full adder using Single Electron Transistor. It is simulated using SIMON which is IEEE standard and the results are observed. The stability analysis for the circuits designed is also done and the stability plots are obtained using SIMON. The circuits designed are found to be stable.

Keywords: SET, SIMON, Stability Plot, Coulomb Blockade

I. INTRODUCTION

One of the extraordinary creations of the 20 th century is the semiconductor transistor. The discovery of the transistor has clearly had enormous impact upon our lives and work. Over the past 30 years, silicon technology has been following Moore's law according to which the density of transistors on a silicon integrated circuit doubles about every 18 months. The last decade has seen a startling shrinkage in the feature size of MOS based circuits and an upsurge in the number of transistors [2].

Recent applications of transistors in the fields of computer technology and other electronics, requires further size reduction. This means not only smaller devices but also low power consumption and better electronic properties. The ever decreasing feature size, and the alternatively increase in the number of transistors per mm2, enhanced the vast improvements in semiconductor based designs.

However, the transistor cannot be shrunk below some limit due to some problems emerging when the size of the fabricated transistors shrink. When transistors are shrunk below 100 nm of size some new quantum mechanical effects become significant. Tunneling effect Increases in a device with very large transistor density which causes crosstalk between transistors built next to each other. The smaller size of n or p doped regions can lead to tunneling of electron form one electrode to the other resulting a reduced ability of control. Furthermore fabrication techniques of small devices are more complicated and need to be more accurate. Thus there is a need of newly designed devices and fabrication methods that can operate in smaller sizes.

With the anticipated end of the CMOS era, several successor technologies based on alternative operating principles and greater scaling potential have been under investigation for the last two decades. Some of the successor technologies are Single Electron Tunneling (SET), Rapid Single Flux Quantum (RSFQ), Magnetic Spin devices, Resonant Tunneling Diodes (RTD) and Carbon Nanotubes.

A promising technology to succeed CMOS is Single Electron Tunneling (SET) technology, as it does not suffer from the limitations faced by CMOS technology (power consumption and scalability). SET technology allows the control of single or few electrons and therefore has potential to perform computation with ultra-low power consumption. The quantum mechanical behavior

increases with downscaling of feature sizes, especially when reaching the nanometer region. This causes problems for CMOS, whereas for SET, which is based on quantum mechanical principles, this results in improved device behavior. Consequently, SET technology is scalable to the nanometer region and beyond. SET technology is fundamentally different from CMOS as it is based on tunneling of electrons. This difference opens up avenues for new technology, which try to effectively use the basic SET properties.

II. CONSTRUCTION OF THE SET

The single-electron transistor describes a single electron transport through a quantum dot. A quantum dot is a semiconducting nanoparticle whose electrons are confined in all three spatial dimensions. There are many variations to the structure of the single-electron transistor. The main components of the single- electron structure are shown in fig. 1.

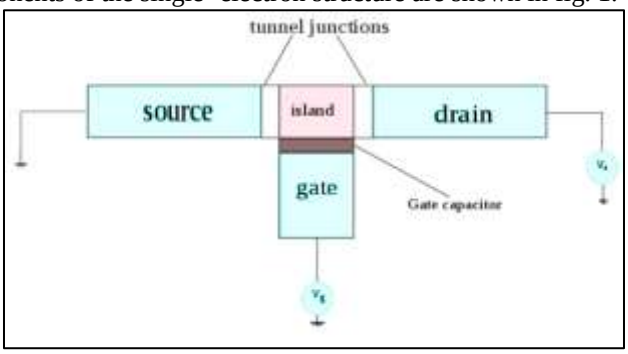

Fig. 1: Structure of SET

The island represents the quantum dot which is connected to the drain and source terminals. Electron exchange occurs only with the drain and source terminals, which are connected to current and voltage meters.

The gate terminal provides electrostatic or capacitive coupling. When there is no coupling, there is an integer number N of electrons in the quantum dot (island). The total charge on the island is quantized and equal to qN. (Since tunneling is a discrete process, the electric charge that flows through the tunnel junction flows in multiples of the charge of electrons e).

III. COULOMB BLOCKADE

As discussed earlier SET consists of a metal island, coupled to two metal leads via tunnel barriers. At temperatures below 1 K, no current can pass through the island with low bias voltage. This effect is known as the Coulomb blockade, which is the result of the repulsive electron–electron interactions on the island. Coulomb blockade is the repelling energy of previous electron present in the island to the next electron coming towards the island. The concept of Coulomb blockade refers to the phenomenon that tunneling through an island may be inhibited at low temperatures and small applied voltages. The reason is that the addition of a single electron to such a system requires an electrostatic charging energy.

IV. ELECTRON TUNNELLING

Tunneling refers to the ability of using the quantum wave properties of an electron to allow transmission through a thin voltage-potential barrier. According to the laws of classical electrodynamics, no current can flow through an insulating barrier. But quantum mechanics says that there is a finite probability for an electron on one side of the barrier to reach the other side. When a bias voltage is applied, there will be a current. This tunneling current will be proportional to the bias voltage. In electrical terms, the tunnel junction behaves as a resistor with a constant resistance. An arrangement of two conductors with an insulating layer in between not only has a resistance, but also a finite capacitance. The insulator is also called dielectric in this context; the tunnel junction behaves as a capacitor.

We know that for two conductors separated by an insulator, charge and voltage are proportional.

$$Q = CV$$

Where Q is the charge on the conductors, C the capacitance and V is the voltage between the conductors. The electrostatic energy stored in the conductors is given by

$$E = \frac{1}{2}CV^2 = \frac{Q^2}{2C}$$

The total energy E depends on the amount of charge on the capacitor and on the electric potential V.

For an electron to tunnel through the junction, the Coulomb energy $E_c = \frac{{q_e}^2}{2C}$, where C is the capacitance of the tunnel junction and qe is the charge of an electron (1.60217*10-19 C), is at least needed.

V. PRINCIPLE OF OPERATION

As previously discussed Single electron transistor, consists of two tunnel junctions sharing one common electrode with a low self-capacitance, known as the island. The electrical potential of the island can be tuned by a third electrode (the gate), which is capacitively coupled to the island.

In the blocking state no accessible energy levels are within tunneling range of the electron (red) on the source contact. All energy levels on the island electrode with lower energies are occupied. When a positive voltage is applied to the gate electrode the energy levels of the island electrode are lowered. The electron can tunnel onto the island, occupying a previously vacant energy level. From there it can tunnel onto the drain electrode. The energy levels of the island electrode are evenly spaced with a separation of ΔE. ΔE is the energy needed to each subsequent electron to the island, which acts as a self-capacitance C. The lower C the bigger ΔE gets. Fig. 2 shows energy band before and after modifying the gate voltage of a SET transistor (blockade state / open state).

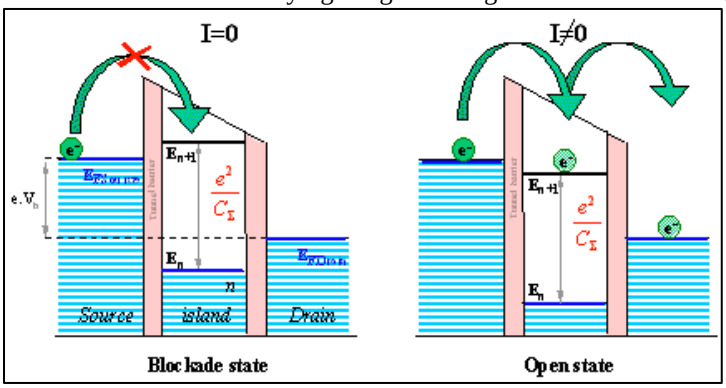

Fig. 2: SET operating principle

In order to observe coulomb blockade effects, there are two necessary conditions:

The charging and discharging of tunnel junction and thermal fluctuations are closely related to each other. Since, the thermal fluctuations can disturb the motion of the electrons and can suppress the quantization effects. To avoid this problem, coulomb energy must be greater than the thermal fluctuations. Thus, the required condition to observe the single electron phenomenon is as follows:

$$E = \frac{e^2}{2C} > K_B T$$

Where kB is Boltzmann's constant and T is temperature in Kelvin.

In classical theories an electron was assumed to be well localized. However, in the quantum mechanics theory electrons are described by wave functions, indicating the probability of the presence of an electron. If a tunnel barrier is insufficiently opaque the electron wave function extends through the barrier and the electron is not clearly localized on either site of the tunnel junction. The opaqueness of a tunnel barrier is described by the tunnel resistance Rt. A sufficient condition for observing SET charging effects is:

$$R_T > \frac{h}{e^2} = 25.813\ k\Omega$$

Where h is plank's constant and e is electronic charge. The quantity ħ/e2 is called the quantum resistance or quantum conductance (G= 38.74μS).

The formulation of the Coulomb blockade model is only valid, if electron states are localized on islands. If the tunnel barriers are insufficiently opaque, it is not possible to localize electrons on a quantum dot. Only if the tunnel barriers are opaque enough they will constrain electrons to be confined within a certain volume. The tunneling junctions or the barriers are made thick enough so that the electrons exist in the island, source, or drain, such that the quantum fluctuation in the number N due to tunneling through the barrier is much smaller than one.

By sweeping the gate voltage, the build-up of induced charge will be compensated in a periodic interval due to the tunneling of discrete charges. The competition between the induced charges and the discrete compensation leads to so-called Coulomb oscillations as shown in fig. 3.

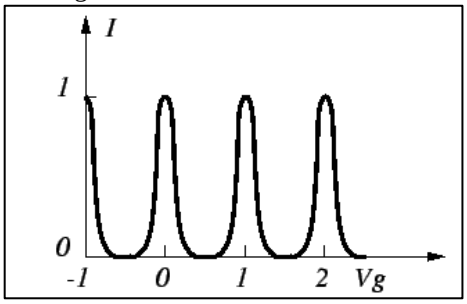

Fig. 3: Coulomb oscillations

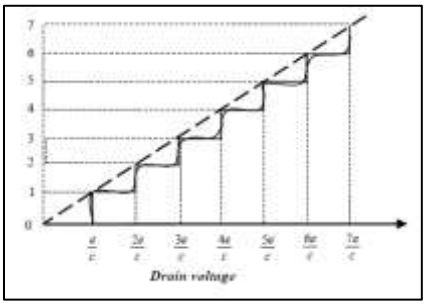

Fig. 4: Coulomb Staircase

Consider that the gate voltage is fixed for the single-electron transistor while the drain-source voltage is varied. The current-voltage results exhibit a staircase-like behavior known as a Coulomb stair-case and is shown in Fig. 4.

VI. SET BASED FULL ADDER

Binary addition is greatly used in almost all arithmetic operations. In computers it is also used in calculations related to memory access such as index based addressing. When dedicated hardware is not available for multiplication and division operations repeated addition operations are performed. Furthermore, for implementation of more complex arithmetic operations, such as polynomial approximations adder can be used as a building block. Thus for overall system performance, the implementation of addition operation efficiently is of great prominence.

The most commonly used component for implementing addition operation is a Full adder (FA). The operation of full adder can be summarized in truth table which is shown in Table-1.

There are several different ways to implement a Boolean gate based FA .Figure 5 shows an FA implementation that is optimized for gate level delay.

Table-1
Operation of full adder

C_{i-1}	A_i	B_i	C_i	S_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

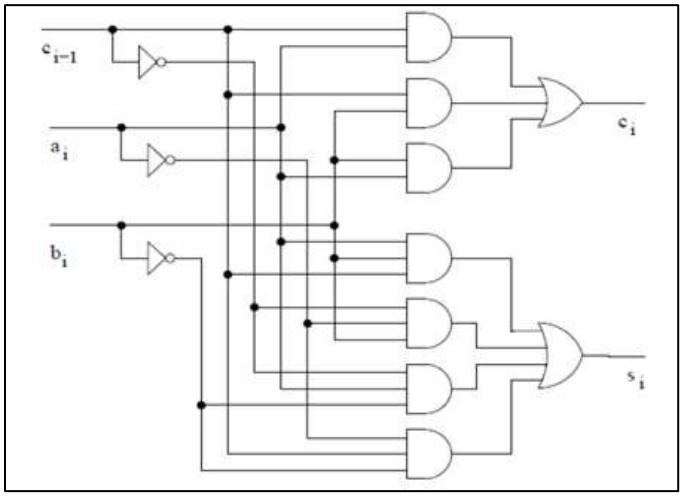

Fig. 5: Logic diagram of AND/OR gate Based full adder

The single electron full adder is shown in Fig. 6. The circuit comprises of 185 islands N1, N2, N3….N185 bounded by 89 tunnel junctions. The capacitance of J junctions is 0.1x10-18F and their resistances are 1x105 Ohm. The voltage V_{dd} is constant and its value 16 mV. Table-2 shows the circuit parameters of the Boolean gates used in FA.

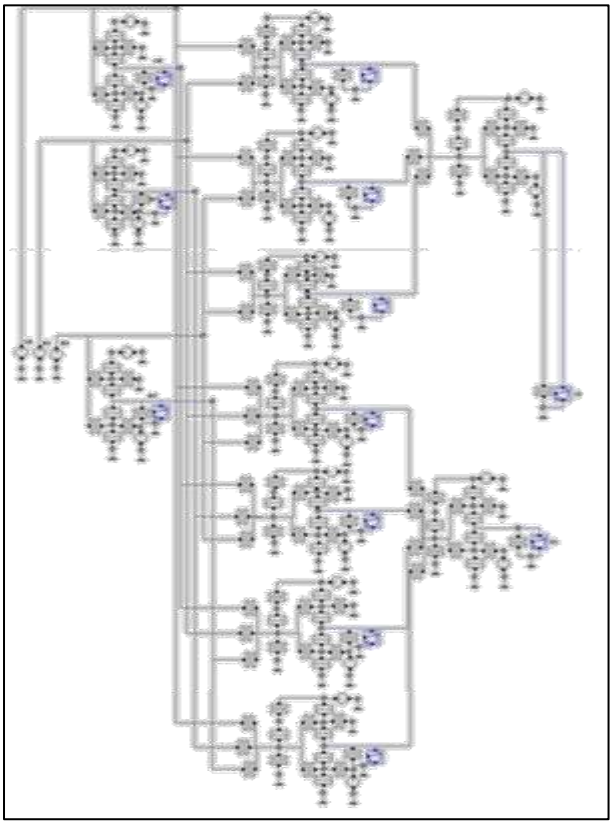

Fig. 6: Circuit of Full Adder using SET

Table - 2
Circuit parameters for FA Boolean Gates

Gate	Cn	Co	Cb
2-input AND	0.3aF	8.4aF	12.4aF
3-input AND	0.3aF	8.1aF	13.4aF
3 input OR	0.3aF	8.1aF	11.6aF
4 input OR	0.3aF	7.8aF	11.6aF

VII. SIMULATION RESULT OF FULL ADDER

The simulation result of full adder is shown in figure 7. C0 is the carry input and A1 and B1 are the inputs to the adder. C1 and S1 represents the carry and the sum outputs. The stability plot for full adder circuit implemented is shown in figure 8. The points that correspond to the input control signal vectors [0, 0], [0, 1], [1, 0] and [1, 1] are marked as A, B, C and D respectively in the stability plots.

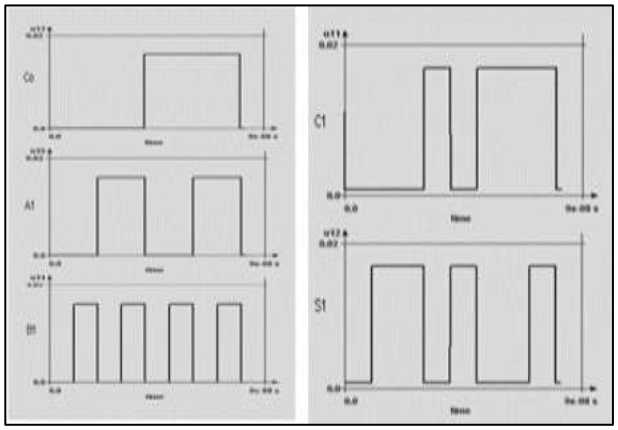

Fig. 7: Simulation result of Full Adder

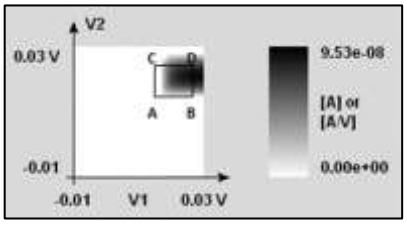

Fig. 8: Stability plot

VIII. APPLICATIONS OF SET

The applications of SET are listed below:

- They are used as supersensitive electrometers due to their high sensitivity. Absolute measurements of extremely low dc currents (~10-20A) have been demonstrated.
- One of the most important application of single-electron electrometry is the possibility of measuring the electron addition energies (and hence the energy level distribution) in quantum dots and other nanoscale objects.
- The single-electron transistor can also be used to detect infrared signals at room temperature.

IX. CONCLUSION

This paper focuses on theoretical discussion of basic principles of Single Electron transistor, its applications and its importance in the field of nanotechnology to provide ultra-low power consumption and high operating speed. The full adder is designed and simulated using SIMOPN. The stability analysis for the circuits designed is also done and the stability plots are obtained using SIMON. The circuits designed are found to be stable.

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