Realization of Multiplier Architecture Based on VHBCSE Algorithm for Reconfigurable FIR Filter using Verilog HDL

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Abstract

FIR filter with reconfigurability is the significant component in the advanced SDR (software defined radio) application. Complexity and power consumptions are the two factors that must be consider while designing re-configurable fir filter. Proposed VHBCSE algorithm searches for 2-bit CSE vertically across adjacent coefficients at first. Then variable 4-bit and 8-bit CSE is applied horizontally within each coefficient. The VHBCSE algorithm based multiplier design reduces number of adders and switching activity of the multiplier adder block. A 4 tap FIR filter is implemented and the design shows that VHBCSE algorithm based multiplier gives better performance and reduced power consumption and area compared to that of existing fixed 2-bit and 3-bit BCSE technique. The design for reconfigurable fir filter based on VHBCSE algorithm is coded in Verilog, synthesized and simulated in Xilinx ISE Design Suite 14.7 tool.

Keywords: BCSE algorithm, Reconfigurable FIR Filter, SDR system, Shift and add technique, VLSI design

I. INTRODUCTION

Digital filters play an essential role in analog and digital communication. The purpose of using fir filter is to eliminate unwanted signal and providing better quality of signal component at the output. FIR filters are widely used in wireless communication as channel equalization and it is the fundamental component in biomedical and in image device as it is used as the noise suppression. In literature many algorithms have been proposed to implement efficient, low cost, low complexity multiplier architecture for FIR filter.

The earlier proposed algorithms are divided into graph based technique and common sub expression technique. Though these two approaches provide efficient multiplier architecture by running these algorithms on a fixed set of coefficients for a fixed amount of time on a highly computing platform but it is not applicable for application like SDR whose filter coefficients vigorously changes based on the specification of different standard in a computing platform. Thus many researchers have contributed towards realizing fir filter with reconfigurability and binary common sub expression elimination (BCSE) is one of those algorithms. BCSE method is used for designing multiplier which is applicable for reconfigurable fir filter with reduced hardware. This method eliminates the redundant patterns that are present in the binary representation of filter coefficients. The length of the BCSs is the main factor that needs to be considered because as the length of BCSs increases adder step as well as hardware cost also increases, which makes the filter design inefficiency.
II. EXISTING METHOD

The existing fixed BCSE algorithms eliminate the redundant computation vertically by considering 3-bit or 2-bit binary common sub expression present across the adjacent coefficients. Horizontal BCSE algorithm utilizes CSs occurring within each coefficient to get rid of redundant computations, while vertical BCSE uses CSs found across adjacent coefficients to eliminate redundant computations. Designing a reconfigurable fir filter based on existing method i.e. fixed length (2 bit and 3 bit) BCSE faces several problems they are; BCSE algorithm follows signed magnitude format for input and coefficients of the filter, whereas most of the system supports signed decimal format for representation which got wide range of application. Also the convention method completely ignores the optimization of multiplier adder tree (MAT) in the filter design. Also in the convention method BCSE algorithm is applied only in the 1st layer thus adders are used to add up the partial products this leads to increase in hardware also power consumption. Though BCSE technique reduces the redundant computation and improves the performance, this method consumes large area and power.

III. PROPOSED METHOD

The figure 2 shows the work flow of a multiplier design using VH-BCSE algorithm. Here the multiplier design takes input length as 16bit and length of the filter coefficient as 17 bit where 17th bit indicates the sign. The final result i.e. output length is considered to be 16 bit. The inputs which are sampled are loaded to the register whereas in LUT the filter coefficients are stored.

As shown in figure 2 at first coefficients are given to the sign conversion unit based on the MSB bit of the coefficients, this block produces either inverted or original multiplexed coefficient (MC). These multiplexed coefficients are then given to the partial product generator (PPG) unit to which input is also given. The PPG unit produces partial product which are summed up in the following layer. The data which is obtained from the partial product generator block is appropriately chosen by the multiplexer unit. Control logic generator block which gives control signals and these signals are given to the layer 2 and 3 where additions of the PPs are performed in a controllable manner. And the final multiplication result is obtained from the layer 4 and it is given to sign conversion block which gives either complemented or original result based on MSB bit. Finally in the register the result of the multiplication is stored.
A. Steps Involved in the VHBCSE Algorithm:

- Get the input of 16-bits (X [15:0]).
- Store coefficients of 17-bits (H [16:0]) in LUT.
- Take 1’s complement of the 16-bits (except the MSB) coefficient (H'[15:0]).
- If the MSB, the 17th bit (H [16]) of the coefficient is 1, then choose the complemented version of coefficient.
- Partition the multiplexed coefficient (MC) (Hm[15:0]) into fixed groups of 2 bits each.
- Partition the MC into groups of 4 bits each based on the control signal obtained from the control logic generator unit.
- Compare the result.
- Partition the MC into fixed group of 8-bit and compare the result based on the control signal.
- Obtain the final addition result by performing 1-bit right shift on the output.
- Take 2’s complement of the output, if the MSB the 17th bit (H [16]) of the coefficient is 1, then choose the complemented version.
- Multiplication is completed. Store this result, H*X, in the register.

Fig. 2: Work flow chart of constant multiplier based on VH-BCSE algorithm

Fig. 3: Block diagram of proposed multiplier design with reconfigurability
IV. FIR FILTER ARCHITECTURE

The FIR filters performance is defined by its multipliers hence in any fir filter, multipliers plays a crucial role. To improve the performance of the fir filter one must concentrate on the multiplier architecture design because it consumes more area as well as power. VHBCSE algorithm based multiplier gives better performance and less power consumption compared to the other existing method. A 4 tap fir filter is implemented based on VHBCSE technique. Figure 4 shows a 4 tap fir filter with coefficients h0, h1, h2, h3 each of 16bit length and a variable input X of 16 bit length.

![Fig. 5: A 4 tap fir filter design](image)

V. RESULT

![Fig. 5: RTL schematic of VHBCSE based Multiplier design](image)  
![Fig. 6: RTL schematic of 4 tap fir filter based on VHBCSE algorithm](image)
VI. CONCLUSION

The multiplier architecture based on proposed algorithm is far better than that existing fixed bit algorithm in terms of area and power utilization. The hardware circuitry is reduced due to the reduced switching activity of multiplier adder block compared to existing method. Also a 4 tap fir filter based on VH-BCSE algorithm multiplier is implemented. This implementation result shows that vertical horizontal based multiplier architecture is best substitute in terms of efficiency for higher and lower order fir filter design.

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REFERENCES