Implementation of High Speed and Energy-Efficient Carry Skip Adder using Verilog HDL

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Abstract

This paper presents a high speed carry skip adder (CSKA) structure yet brings down energy utilization contrasted with the existing one. The proficiency is improved that of the existing CSKA (Conv-CSKA) structure with updating the adder by applying the concatenation and incrementation plan. The AND-OR-Invert (AOI) and moreover OR-AND-Invert (OAI) logic gates are utilized for the skip logic as a replace to the multiplexer logic. The structure is acknowledged in both uniform (FSS) where at long last the speed and energy parameters of the adder are updated. At long last, a hybrid variable latency expansion of the proposed structure with an Brent-Kung parallel prefix adder, which brings down the power utilization without extensively affecting the speed, is presented. The proposed structures are evaluated by comparing their speed, power and energy parameters with those of different adders design by Verilog HDL and Simulated by Modelsim 6.4 c and Synthesized by Xilinx Design Suite 13.2 and proposed system implemented in FPGA Spartan 6 XC6SLX4 TQG-144 with a speed grade of -3.

Keywords: Carry Skip Adder (CSKA), Energy Efficient, High Performance, Hybrid Variable Adders, Voltage Scaling

I. INTRODUCTION

Adder is the fundamental block in any arithmetic and logic units (ALUs) and majority of digital signal processing (DSP) application, used to perform a number of operations such as subtraction, multiplication, division, and address computation as well as additions. Addition is a basic operation for any advanced digital system.

The CSKA is fast but the conventional CSKA consumes large area and power. Hence designers have to use different approaches in order to reduce the power and area. In majority of the work reviewed so far, the attention was on the speed, while the power utilization and area usage of CSKAs where not considered. As the conventional CSKA has multiplexer based skip logic, form a greatest part of basic critical path delay of adder, which is not been lessened. So that delay is adjusted by joining concatenation and incrementation scheme to conventional CSKA. The modification provides us with the simple carry skip logic based on the AOI/OAI compound gates instead of multiplexer for enhancing the speed and energy, and replacing some of the middle stages in its structure with PPA which lowers the power consumption.

II. CONVENTIONAL CARRY SKIP ADDER

Fig. 1: Block Diagram of Conventional Structure of CSKA.
The existing CSKA structure comprises of a RCA blocks and the 2:1 multiplexer logic [1]-[2] is as shown in the Fig.1. The 2:1 multiplexer acts as interconnection between the RCA blocks in each stage, that placed into one or more level structures. In each stage of Conventional CSKA, the number of FAs has greater influence on the speed of a adder. In this method the area and power is not been reduced and only the speed has increased and also the delay of the skip logic and adder critical path delay is not reduced.

III. PROPOSED CI-CSKA

The proposed fixed stage CSKA with concatenation and incrementation scheme [3] with the modification to the conventional CSKA is shown in Fig. 2. Hence it is written as CI-CSKA. The multiplexer is replaced by the AOI and OAI skip logic in the CI-CSKA structure. Since the modified skip logic has less number of transistors, the reduced area, delay and smaller power consumption compared to the existing multiplexer skip logic [4]. The carry output of the even stages is complemented since the carry get complemented when the carry propagates through the skip logic in the proposed structure.

![Fig. 2: Proposed CI-CSKA Adder Structure.](image)

IV. PROPOSED HYBRID VARIABLE LATENCY CSKA

A. Variable Latency Adder Depend on Adaptive Clock Stretching

The path with maximum delay will be generated rarely in adder having dynamic latency [5]. Henceforth without diminishing the clock frequency, the supply voltage might be lessened. One and only clock cycle is sufficient for finishing the operation, if the critical path are initiated. If not two clock cycles are required for completing the operation. The xor logic operation of the input bits i.e. predictor block is used to identify the critical path. The difference of path having maximum and minimum delay is used to decrease the voltage.

B. Hybrid Variable Latency CSKA

The proposed CI-CSKA, is added with the variable latency adder feature by replacing last two stages of the CI-CSKA with parallel prefix adder as shown in Fig. 3. The parallel prefix adder is used to decrease the delay of the lengthiest path. Along these lines, the increase in the accessible slack time in the variable latency structure with the utilization of the quick PPA. In the proposed CSKA, the prefix system of the Brent-Kung adder is utilized.

C. Parallel Prefix Brent Kung Adder

The benefit of this looked at other prefix system is that, in this kind of adder the longest carry is figured first than that of the intermediate carry, which are processed by in reverse ways. The another favorable position is that fan-out of this adder is not exactly the other parallel adders, since the length of its wiring is littler. It has basic layout. Here the extent of parallel prefix system is expected as 8 (i.e. Mp = 8).
V. RESULT

Fig. 3: Proposed Hybrid Variable Latency CSKA Adder Structure.

Fig. 4: Comparison graph showing area of various CSKA architecture.

Fig. 5: Delay of CSKA

Fig. 6: Power of CSKA.
VI. CONCLUSION

In this paper the fixed stage size CSKA structure called CI-CSKA was proposed, which displays a higher speed and lower vitality utilization contrasted and those of the conventional one. The speed upgrade was accomplished by altering the structure through the concatenation and incrementation systems. The AOI and OAI basic gates are used to reduce the delay in the existing carry skip adder. In order to reduce the power the CI-CSKA adder is exploited with an altered parallel adder structure at the Last stage for expanding the slack time, which gave us with the chance to bringing down the energy utilization by lessening the supply voltage called hybrid variable latency CSKA.

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REFERENCES