Pulse Triggered Flip-Flop Design with Signal Feed through Scheme using Conditional Pulse Enhancement Technique

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Abstract

A low power pulse triggered flip-flop with signal feed through scheme using Conditional Pulse Enhancement technique is presented in this paper. The proposed design adopts a modified True Single Phase Clock Latch structure and employs a signal feed through scheme to enhance the delay. The long discharging path problem in conventional explicit type pulse triggered flip flops are successfully solved through this method. In order to further enhance the speed and power performance, a conditional pulse enhancement technique is employed at the discharging path. Post layout simulation results based on TSMC 180 nm technology reveals that proposed flip flop features better power delay product when compared to conventional flip flops like ep-DCO, CDFBF, SCDFBF, MHLFF, SCCER and flip flop based on signal feed through scheme.

Keywords: Conditional Pulse Enhancement, Flip-Flop (FF), Low Power, Pulse-Triggered, Signal Feed through

I. INTRODUCTION

In all digital circuits flip flops are the critical timing elements used and have a large impact on circuit speed and power consumption. In order to determine the efficiency of the whole synchronous circuit, the performance of flip flop is very important. In all kinds of digital designs, flip flops are the most extensively used basic storage elements. Intensive pipelining techniques are often adopted by digital designs nowadays and many Flip flop (FF) -rich modules are employed such as register file, counters, shift registers etc. The total power consumption of the clock system which consists of storage elements as well as the clock distribution networks is as high as 50% of the total system power. Thus a significant portion of the chip area and power consumption is contributed by the FF’s to the overall system design [1], [2].

Master-slave and pulse-triggered flip-flops are selectively used by many contemporary microprocessors [3]. Pulse-triggered flip-flops are defined by their soft edge property which reduce the two stages into one stage. Inside these pulse-triggered flip-flops logic complexity and number of stages are reduced, leading to small data -to-Q delays. As a result of the zero or even negative setup time, pulse-triggered flip-flops allow time borrowing across cycle boundaries. Pulse-triggered flip-flops provide higher performance than their master-slave flip flops due to these timing issues.

When compared to conventional master-slave based FF’s and Transmission Gate (TG) FF’s, Pulse Triggered Flip flops (P-FF) are more popular because of its single-latch structure. The circuit simplicity also lowers the overal power consumption of the clock tree system. A pulse triggered flip flop basically consists of a latch and a pulse generator. A pulse generator is used to strobe signals and a latch is used for data storage. A latch acts like an edge triggered FF, if the pulses triggered are sufficiently narrow. A pulse triggered flip flop is simpler in its circuit complexity since only one latch is required as compared to two in the conventional master slave configuration. Across clock cycle boundaries, pulse triggered flip flops results in time borrowing and feature a negative setup time or zero. In order to cope with possible variations in signal distribution network and process technology, pulse generation circuitry requires delicate control of pulse width. Design space exploration is a widely used technique in order to obtain balanced performance among delay, power and area [4]-[6].

In this brief, a pulse triggered flip flop with signal feed through scheme using conditional pulse enhancement technique is presented in this paper. By feeding the input signal directly to an internal node of the latch, longer delay is shorten in order to speed up the data transition. A simple pass transistor is introduced for extra signal driving. In order to further enhance the speed and power performance, a conditional pulse enhancement technique is employed at the discharging path. A new pulse triggered flip flop design is formed with improved speed and Power Delay Product (PDP) performances.

This paper is organized as follows. Section 2 deals with the literature survey of conventional explicit type pulse triggered flip flops and also describes about the proposed flip flop design. Section 3 contains the simulation results of various flip flops and section 4 contains the summary of the paper.
II. LITERATURE REVIEW

A. Conventional Explicit Type Pulse Triggered Flip Flops Designs

Based on pulse generator circuitry-FF’s can be partitioned into explicit or implicit type. The pulse generator and latch are separate in an explicit type pulse triggered flip flop [7]. In case of implicit type P-FF no explicit type pulse signals are generated and pulse generator is a part of latch. In general implicit type P-FF’s are more power economical without explicitly generating pulse signals. But they results in longer discharging path. On the contrary explicit type pulse triggered flip flops results in more power consumption but it provides a unique speed advantage because of the logic separation from the latch design. When one pulse generator is shared between a group of FF’s its circuit complexity and power consumption can be effectively reduced. Some existing explicit type P-FF’s are reviewed first in order to provide a comparison.

Explicit type Data-Close to-Output (ep-DCO) P-FF design is shown in fig.2 (a). ep-DCO design consists of a semi dynamic True-Single-Phase-Clock (TSPC) structured latch design and a NAND logic based pulse generator [7]. In this P-FF design, in order to hold the internal node X, inverters I2 and I1 are used and to latch data inverters I4and I3 are used. The delay of three inverters determines the pulse width of the pulse generator. In this design on every rising edge of clock, the internal node X is discharged in presence of a static input ‘1’. Initially when the pulse is ‘LOW, which turns the transistor “MP1” ON and the node “X” is charged. When data is high at the rising edge of the clock, node X discharges. This continuous discharge of node X results in large switching power dissipation. This was a serious drawback of this design and as a result it leads to large switching power dissipation. So in order to overcome the drawback of this design, various techniques were introduced such as conditional discharge, conditional capture, and conditional precharge and conditional pulse enhancement scheme [8]-[12]. A Conditional Discharged Flip flop (CDFF) is shown in fig.2 (b). In this design if the input data remains ‘1’ no discharge occurs since the output signal Q_fdbk controls an extra NMOS transistor N5[10]. Three stacked transistors N3-N4-N5 are present in this design which results in worst case delay.

A Static Conditional Discharge flip flop (SCDFF) is shown in fig.2(c). A static latch structure is used here. In this design, from periodical precharges, node X is exempted. When compared to CDFF design, a longer data-to-Q (D-to-Q) delay is produced. In both the above designs three stacked transistors are present in the discharging path i.e., N1-N2-N3 which results in worst case delay. A powerful pull-down circuitry is needed, in order to overcome this worst case delay for better speed performance which leads to extra power consumption and layout area [11]. The main structure of the SCDFF consists of two static stages. By eliminating the precharging at node X, this flip flop reduces the internal switching activity and utilises the inverted output “Qbar” as a discharge control signal. This helps to reduce the power dissipation, regardless of the input data activity. To reduce the capacitive load at node “X”, it operates only the output pull-up transistor “P2” in the second stage. During the sampling period, transistors “N1” and “N4” are turned on due to delay incurred by a dual pulse generator, which in turn causes the input “D” to propagate to the output.

Modified Hybrid Latch flip flop (MHLFF) is shown in fig.2 (d). This flip flop also uses a static latch. At node X, keeper logic is removed when compared to above designs. The output signal Q controls a weak pull up transistor P1 and maintains the level of node X when Q equals 0. The MHLFF design results in two major drawbacks despite its circuit complexity. First a prolonged 0 to 1 delay is expected since node X is not precharged. The delay deteriorates further since at the discharging transistor N3, a level degraded clock pulse is applied. Second in certain cases node X becomes floating and its value may drift causing extra dc power [13]. MHLFF flip flop uses a different pulse generator when compared to that of ep-DCO, CDFF and SCDFF. Instead of using a NAND logic based pulse generator, a pulse generator with three inverters and a NMOS transistor have been used.

Single Ended Conditional Capturing Energy Recovery flip flop (SCCER) is shown in fig.2 (e). The SCCER flip-flop operates in a pre-charge and evaluate phase same as that of a dynamic flip flop [14]. However, for charging the pre-charge node “X”, small pull-up ‘pMOS’ transistor (P1) is used instead of using the clock for pre-charging. For the storage mechanism the SCCER flip-flop uses a ‘NAND’-based latch. Using a feedback from the output to the control transistor “N3”, the conditional capturing was implemented. Therefore, the evaluation paths is turned off if the state of the input data is same as that of the output, Preventing
the node from being discharged. When input data remains idle for more than one clock cycle which results in power saving at low data switching. When node “X” gets discharged through four transistors in series. i.e. “N1” through “N4” and when input data is ‘HIGH’ the worst case timing of this design occurs while opposing with pull up transistor “P1”. In order to ensure the proper discharge of node ‘X’, a powerful pull down circuitry is needed. This results in wider “N1” and “N2” transistors.

A pulse triggered flip flop based on signal feed through scheme is shown in fig.2 (f). At internal node, in order to avoid superfluous switching this design employs a conditional discharge scheme and static latch structure similar to that of SCDFF flip flop. This flip flop forms a unique TSPC latch structure [15]. At the first stage of the TSPC latch a weak pull up PMOS transistor, P1 with gate connected to the ground is used. As a result keeper circuit for the internal node X can be saved and pseudo-NMOS logic style design is formed. This design also reduces the load capacitance at node X [14], [16] in spite of its circuit complexity. In this design input data can drive node Q of the latch directly since a pass transistor Nx controlled by the clock pulse is included (signal feed-through scheme). This extra passage provides auxiliary signal from input source to node Q. At the second stage inverter of TSPC latch, a pull up transistor P2 is used. In order to shorten the data transition delay, the node level can thus be quickly pulled high. Discharging path is provided by the pass transistor Nx. At the second stage inverter, the pull down network is completely removed. Extra driving to node Q is provided by the pass transistor Nx during 0 to 1 data transitions and 1 to 0 data transitions at the discharging node Q. When compared to that of SCDFF design, this flip flop consists of a control inverter, charge keeper, a pull down network and a NMOS pass transistor to guide the signal feed through scheme. Through this scheme 0 to 1 delay is boosted and thus reduces the imbalance between fall time and rise time delays. This design shows better delay when compared to all the above designs.
**Proposed Pulse Triggered Flip-Flop Design**

The proposed design uses a conditional pulse enhancement technique at the discharging path along with the signal feed through scheme. The upper part of the latch design is same as that of the flip flop based on signal feed through scheme. In the proposed design a mechanism is employed to conditionally enhance the pull down strength when input data remains ‘1’. A two input pass transistor logic (PTL) based AND gate is formed at the discharging path when transistor N3 is in conjunction with additional transistor N4 in order to control the discharge of transistor N5. Here the output node Z is zero at most of the time since the AND gate logic inputs are complementary except during the transition edges of the clock. At node Z, temporary floating is harmless during falling edges of the clock when both the input signals equals to ‘0’. When both transistors N3 and N4 are turned ON at the rising edges of the clock, a weak logic high is passed to node Z which then turns on transistor N5 in which time span is defined by the delay inverter I1. At node Z, switching power can be reduced due to diminished voltage swing. The proposed design boosts up the operation of pulse generation circuitry due to parallel conduction of two NMOS transistors (N3, N4). Discharge control signal is driven by single transistor same as that of MHLFF design.

In this design, when a clock pulse arrives, ON current passes through the pass transistor which keeps the input stage of the flip flop from any driving effort when the input data and node Q are at the same level. At node X, pull down path is OFF since the input data and Q_fdbk assume complementary signal levels. As a result no signal switching occurs in any internal nodes. In order to turn on transistor P2, node X is discharged when 0 to 1 data transition occurs which further pulls node Q high.

Through this signal feed through scheme delay can be shortened since from input source via pass transistor a boost can be obtained. Here the pass transistor conducts only for a short period. When a 1 to 0 data transition occurs, pass transistor is turned ON by the clock pulse and by the input stage node Q is discharged. During 0 to 1 data transition, input source shows the discharging responsibility. The loading effect to input source is not significant since pass transistor is turned ON only for a short period. The discharging of input source is lifted when the state of keeper logic is inverted since keeper logic is placed at node Q.

**Design of Universal Shift registers using Proposed Flip Flop**

The circuit diagram of a Universal shift register using Conditional Pulse Enhanced flip flop with signal feed through scheme is shown in fig.2 (h). In this structure conventional pulse triggered flip flop is replaced by the proposed Conditional Pulse
Enhanced flip flop with signal feed through scheme. The internal circuit of each proposed flip flop is shown in Fig.2 (g) Compared to Universal shift register using conventional flip flop, this structure consumes less power and offers a very fast implementation. This universal shift register design can highlight the performance of the proposed FF architecture.

![Image](image-url)

Fig. 2(h): A universal shift registers using proposed Flip-flop design

### III. RESULTS AND DISCUSSION

Through various post layout simulations, the performance of proposed P-FF is evaluated against existing explicit type pulse triggered flip flops. For comparison, five explicit type pulse triggered flip flops were used which include ep-DCO, CDFF, SCDFF, SCCER, MHLFF and flip flop based on signal feed through scheme. In all conventional flip flops except MHLFF and SCCER, CMOS NAND-logic based pulse generator is used. The technology used is Mentor Graphics Eldo with the help of TSMC 180nm CMOS process. The supply voltage used is 1.8V. Sizing of the transistors ensures that pulse generators can function properly in all corners. Each P-FF design is individually subject to product of D to Q delay and power. Input signals are generated through buffers in order to minimize the rise and fall time delays. Table 1 shows the performance comparison of various conventional flip flops and the proposed one. The comparison shows that the proposed design has better power and delay when compared to all the other flip flops. Power Delay Product (PDP) of the proposed design is better when compared to other flip flops.

<table>
<thead>
<tr>
<th>Flip Flops</th>
<th>No: of transistors</th>
<th>D-Q Delay (pS)</th>
<th>Total Power(pW)</th>
<th>PDP (aJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ep-DCO</td>
<td>28</td>
<td>362.79</td>
<td>215.3681</td>
<td>0.078133</td>
</tr>
<tr>
<td>CDFF</td>
<td>29</td>
<td>226.30</td>
<td>257.5204</td>
<td>0.058276</td>
</tr>
<tr>
<td>SCDFF</td>
<td>31</td>
<td>215.94</td>
<td>315.6028</td>
<td>0.068151</td>
</tr>
<tr>
<td>MHLFF</td>
<td>19</td>
<td>226.75</td>
<td>235.5158</td>
<td>0.053403</td>
</tr>
<tr>
<td>SCCER</td>
<td>17</td>
<td>225.40</td>
<td>215.6478</td>
<td>0.048607</td>
</tr>
<tr>
<td>Flip flop with signal feed through scheme</td>
<td>24</td>
<td>189.69</td>
<td>188.0667</td>
<td>0.035674</td>
</tr>
<tr>
<td>Proposed Flip flop with signal feed through using conditional pulse enhancement technique</td>
<td>16</td>
<td>91.824</td>
<td>166.800</td>
<td>0.015316</td>
</tr>
</tbody>
</table>

#### Table - 2

Simulation results of 4-bit Universal Shift register

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Total power(nW)</th>
<th>D-Q Delay (pS)</th>
<th>Flip-flop</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-bit Universal Shift register using Flip flop with signal feed through scheme</td>
<td>1.3909</td>
<td>189.69</td>
<td></td>
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<tr>
<td>4-bit Universal Shift register using proposed Flip flop with signal feed through using conditional pulse enhancement technique</td>
<td>1.3762</td>
<td>91.824</td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2 shows the comparison of 4 bit Universal Shift register using proposed FF and Flip flop based on Signal feed through scheme. Results shows that power consumed by a universal shift register using proposed FF is less when compared to that of universal shift register using flip flop based on signal feed through scheme.

### IV. CONCLUSION

This paper presents a pulse triggered flip-flop with signal feed through scheme using Conditional Pulse Enhancement technique. A signal feed through was provided from input source to internal node of the latch to shorten the transition time and enhance
both speed and power performance. This P-FF design employs a modified TSPC latch structure which consists of a pseudo-NMOS logic and a pass transistor. Conditional pulse enhancement technique was used at the discharging path along with the signal feed through scheme to enhance the speed of the design. In this design a mechanism is employed to conditionally enhance the pull down strength when input data remains ‘1’. A two input pass transistor logic (PTL) based AND gate is formed at the discharging path. Post layout simulations were conducted using Mentor Graphics Eldo with the help of TSMC 180nm technology and the results revealed that proposed design features better power delay product (PDP) when compared to conventional designs like ep-DCO, CDFF, SCDF, MHLFF, SCCER and flip flop based on Signal Feed through scheme.

REFERENCES