Switching Time Table to Generate Triggering Pulses for a Single Phase Diode Clamped Multilevel Inverters

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Abstract

The general function of the multilevel inverter is to get a desired AC voltage from several levels of DC voltages. As the number of voltage levels increases the harmonic content decreases significantly. This paper presents the study of different types of diode clamped multilevel inverters like 3-level, 5-level and 7-level. And also Implemented switching tables to generate triggering pulses for the IGBT switches of diode clamped multilevel Inverters (DCMI). The Simulation results are presented using MATLAB/SIMULINK.

Keywords: Diode Clamped Multilevel Inverter (DCMI), Triggering Pulses, Switching Table, MATLAB/SIMULINK

I. INTRODUCTION

MULTILEVEL inverters have drawn much attention in medium-high voltage and high power applications in recent years [1]. The most popular advantage of the multilevel inverter compared with traditional voltage source inverter are high-power quality waveforms with lower distortion and a low blocking voltage by switching devices. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms [1].Fig.1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor see Fig. 1(a)], while the three-level inverter generates three voltages, and so on [1].

The main multilevel topologies are classified into three categories [4]:

1) diode clamped multilevel inverters
2) flying capacitor multilevel inverters
3) cascaded multilevel inverters

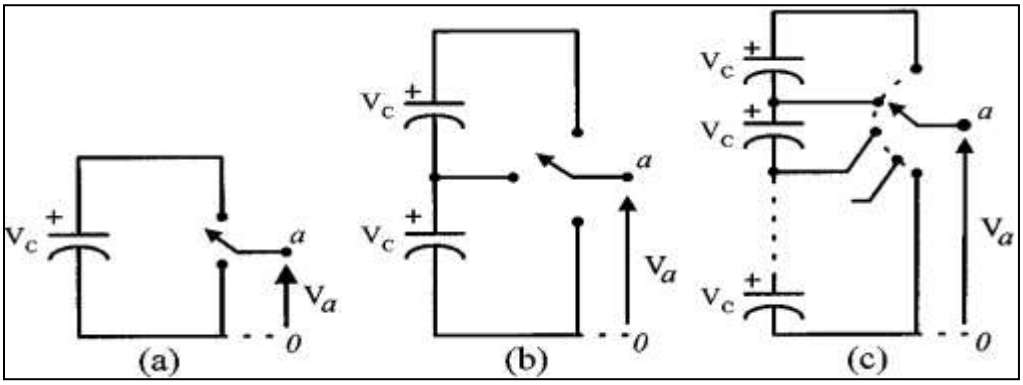

Fig. 1: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

The most widely used multilevel inverter is the diode clamped multilevel inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. This paper presents a study of different types of diode clamped multilevel inverters and also the switching tables to generate triggering pulses for IGBT Switches.

In general the voltage across each capacitor for an N level diode clamped inverter at steady state is $V_{dc}/n-1$. An *n* level inverter needs (*n*-1) voltage sources, 2(*n*-1) switching devices and (*n*-1) (*n*-2) diodes [2]. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform

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II. DIODE CLAMPED MULTILEVEL INVERTERS

A. Three level Diode Clamped Inverter

Fig. 2.1 describes working of a three-level diode-clamped inverter. In this circuit two series-connected bulk capacitors C_1 and C_2 divide the DC-bus voltage. If the middle point of the two capacitors is defined as the neutral point 'n' then the output voltage v_{an} have three states: $V_{dc}/2$, 0 and - $V_{dc}/2$. When switches S_1 and S_2 are turned ON then the output voltage is $V_{dc}/2$.When the switches S_3 and S_4 are turned ON then the output voltage is $-V_{dc}/2$.When the switches S_2 and S_3 are turned ON then the output voltage is 0.The key components that distinguish this circuit from a conventional two-level inverter are diodes D_1 and D_2 [2]. These two diodes clamp the switch voltage to half the level of the DC-bus voltage.

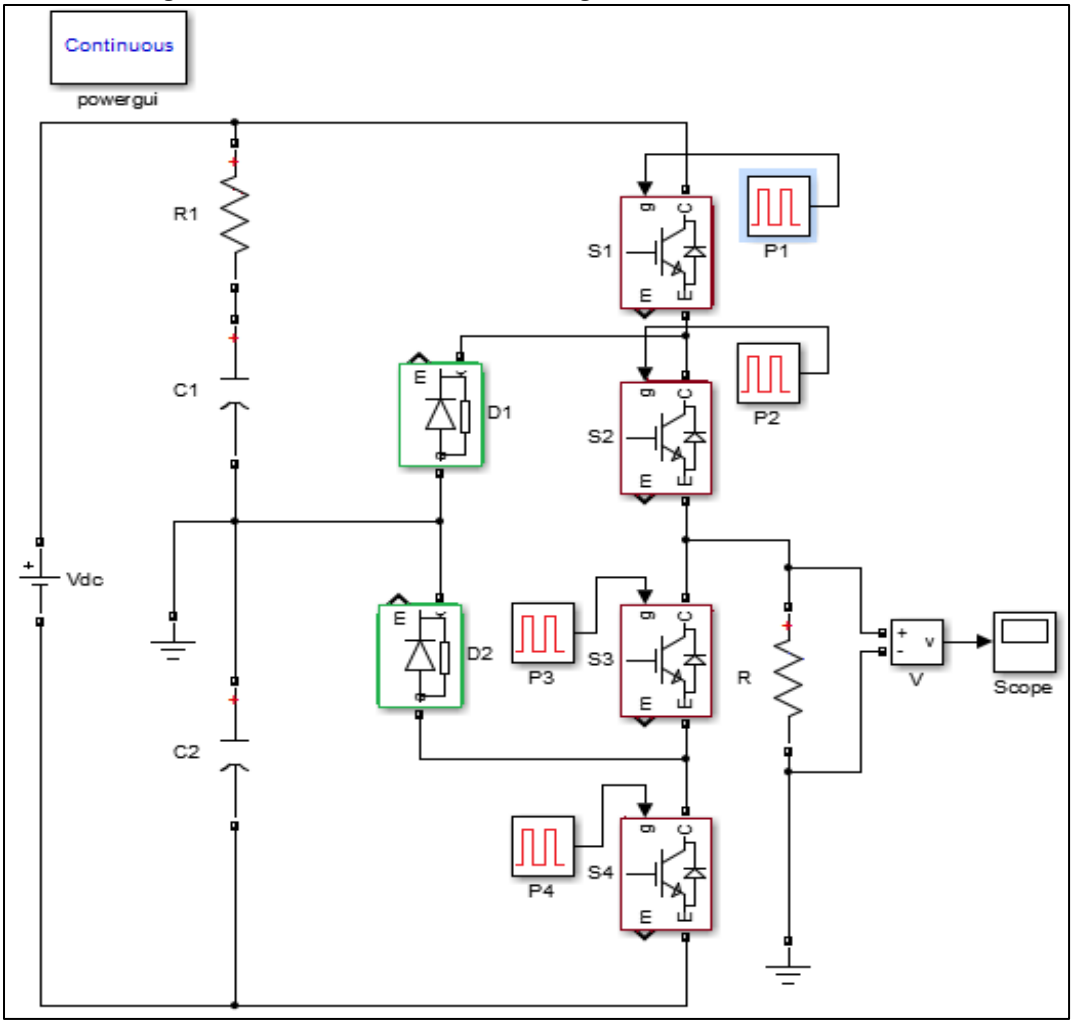

Fig. 2.1: Three level diode clamped inverter

B. Five Level Diode Clamped Multilevel Inverter

Fig. 2.2 shows a five-level diode-clamped multilevel inverter in which the DC bus consists of four capacitors C_1, C_2, C_3 and C_4. For DC-bus voltage V_{dc} the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level i.e. $V_{dc}/4$ through clamping diodes [2].For an output voltage of 0V, two upper switches S_3, S_4 and two lower switches S_5 and S_6 are turned ON. For an output voltage of $V_{dc}/4$, three upper switches S_2, S_3, S_4 and one lower switch S_5 are turned ON. For an output voltage of $V_{dc}/2$, all upper switches S_1 through S_4 are turned ON. To obtain the output voltage of -$V_{dc}/4$, upper switch S_4 and three lower switches S_5, S_6 and S_7 are turned ON. For an output voltage of -$V_{dc}/2$, all lower switches S_5 through S_8 are turned ON.

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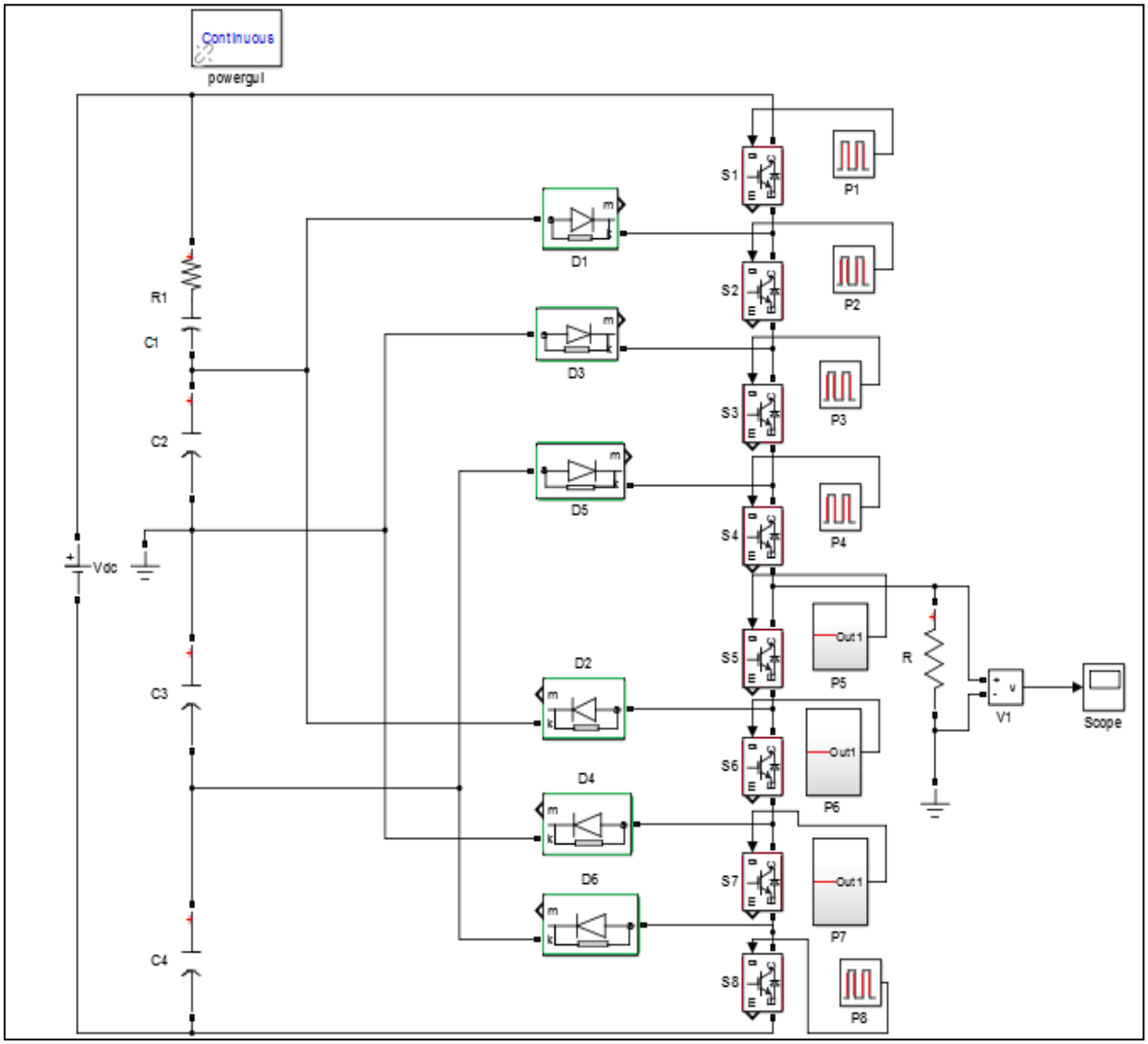

Fig. 2.2: Five level diode clamped multilevel inverter

C. *Seven Level Diode Clamped Multilevel Inverter*

Fig. 2.3 shows a seven-level diode-clamped multilevel inverter in which the DC bus consists of six capacitors C_1, C_2, C_3, C4, C5 and C_6. For DC-bus voltage V_{dc} the voltage across each capacitor is $V_{dc}/6$ and each device voltage stress will be limited to one capacitor voltage level i.e. $V_{dc}/6$ through clamping diodes. For an output voltage of 0V, three upper switches S_4, S_5 and S_6 and three lower switches S_7, S_8 & S_9 are turned ON. For an output voltage of $V_{dc}/6$, four upper switches S_3, S_4, S_5, S_6 and two lower switches S_7 and S_8 are turned ON. For an output voltage of $V_{dc}/4$, fiver upper switches S_2, S_3, S_4, S_5, S_6 and one lower switch S_7 turned ON. For an output voltage of $V_{dc}/2$, all upper switches S_1 through S_6 are turned ON. For an output voltage of $-V_{dc}/6$, two upper switches S_5, S_6 and four lower switches S_7, S_8,S_9, S_{10} are turned ON. To obtain the output voltage of $-V_{dc}/4$, upper switch S_6 and three lower switches S_7, S_8, S_9, S_{10} and S_{11} are turned ON. For an output voltage of $-V_{dc}/2$, all lower switches S_7 through S_{12} are turned ON.

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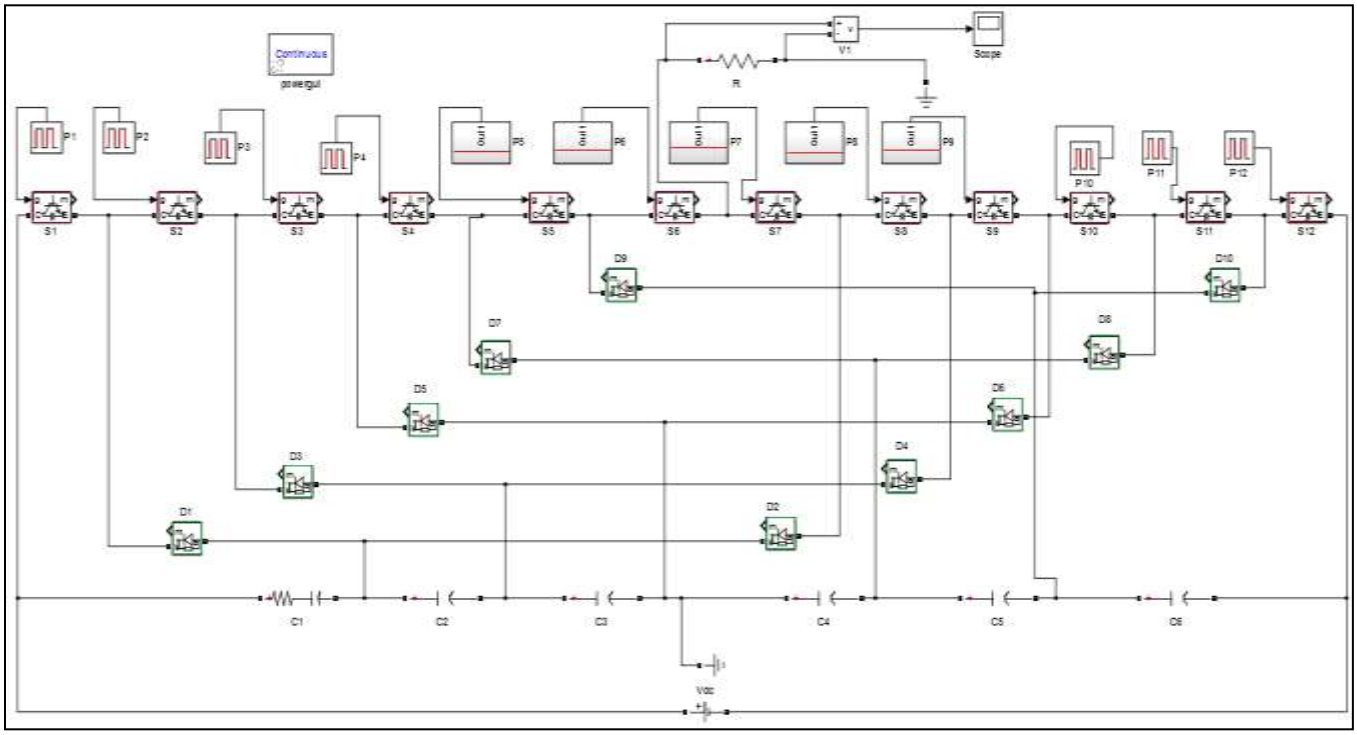

Fig. 2.3: Seven level diode clamped multilevel inverter

III. MATLAB/SIMULINK RESULTS OF DIODE CLAMP MULTILEVEL INVERTERS

A. Three level diode clamped multilevel inverter

Fig 3.1 shows the switching time and angle to generate triggering pulses (P1, P2, P3 and P4) for IGBT switches (S1, S2, S3, S4) of three level diode clamped multilevel inverter [3]. The multi output voltage levels for the DC bus voltage of 100 V are 0V, 50V, -50V.To generate these multi voltages at the output of the Inverter, set the time and pulse width of the pulse generator according to the switching time table shown in Fig 3.1.

VOLTAGE LEVELS	0V	Vdc/2 (50V)	0	-Vdc/2 (-50V)
Time(sec.)	0.005	0.01	0.015	0.02
Angle(Deg.)	90°	180°	270°	360
P1		25%		
P2	PULSE WIDTH 50%			
P3			PULSE WIDTH 50%	
P4				25%

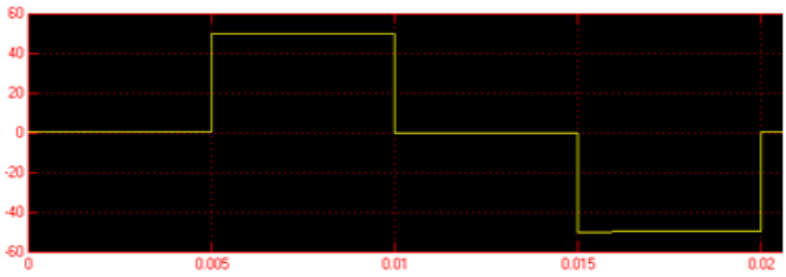

Fig. 3.1: Switching time table and output waveform of three level DCMI

Fig 3.2 shows the total harmonic distortion in the output voltage of three level DCMI for the fundamental frequency of 50 Hz and maximum frequency of 5000 Hz. FFT or Fast Fourier Transform was applied to the output voltage to get the THD result. The total harmonic distortion of 3-level DCMI was computed as 49.39%

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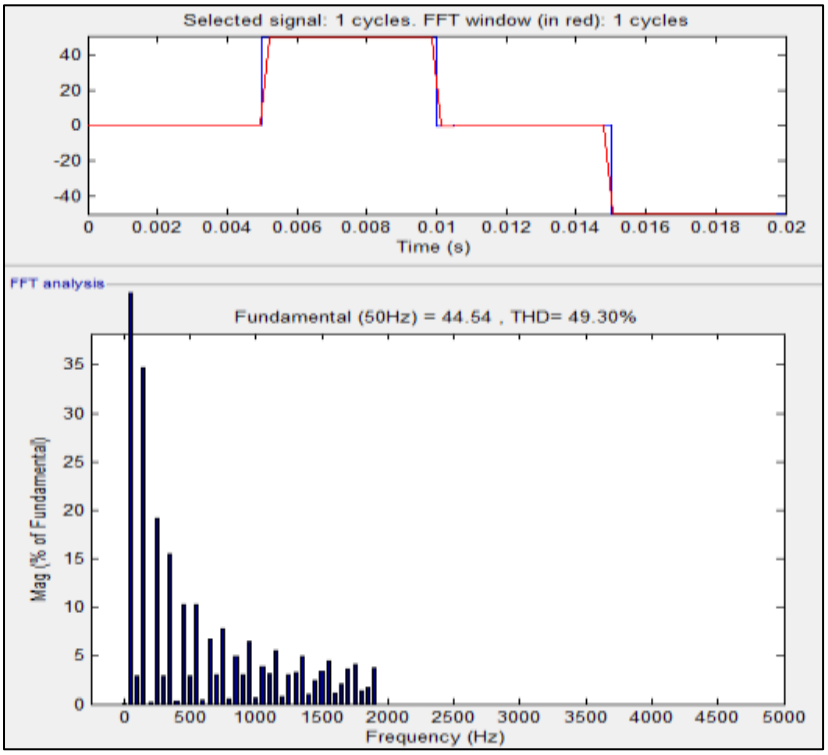

Fig. 3.2: Total harmonic distortion of three levels DCMI

B. Five level diode clamped multilevel inverter

Fig 3.3 shows the switching time and angle to generate triggering pulses (P1 to P8) for IGBT switches (S1 to S8) of five level diode clamped multilevel inverter [3]. The multi output voltages for the DC bus voltage of 100 V are 0V, 25V, 50V, -25V, -50V. To generate these multi voltages at the output of the Inverter, the time and pulse width of the pulse generators are arranged according to the switching time table shown in Fig 3.3

Voltage Levels	0V	Vdc/4 (25V)	Vdc/2 (50V)	Vdc/4 (25V)	0V	-Vdc/4 (-25)	-Vdc/2 (-50V)	-Vdc/4 (-25V)
Time(sec.)	0.0025	0.005	0.0075	0.01	0.0125	0.015	0.0175	0.02
Angle(Deg.)	45^0	90^0	135^0	180^0	225^0	270^0	315^0	360^0
P1			12.5%					
P2		PULSE	WIDTH	37.5%				
P3		PULSE	WIDTH	62.5%				
P4		PULSE	WIDTH	87.5%				
P5						PULSE	WIDTH	87.5%
P6						PULSE	WIDTH	62.5%
P7						PULSE	WIDTH	37.5%
P8							12.5%	

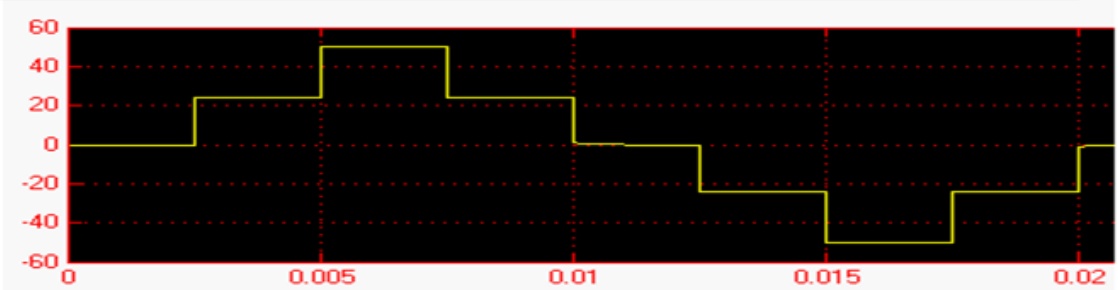

Fig. 3.3: Switching time table and output waveform of five level DCMI

Fig 3.4 shows the total harmonic distortion in the output voltage of five level DCMI for the fundamental frequency of 50 Hz. The total harmonic distortion of 5-level DCMI was computed as 29.60%.

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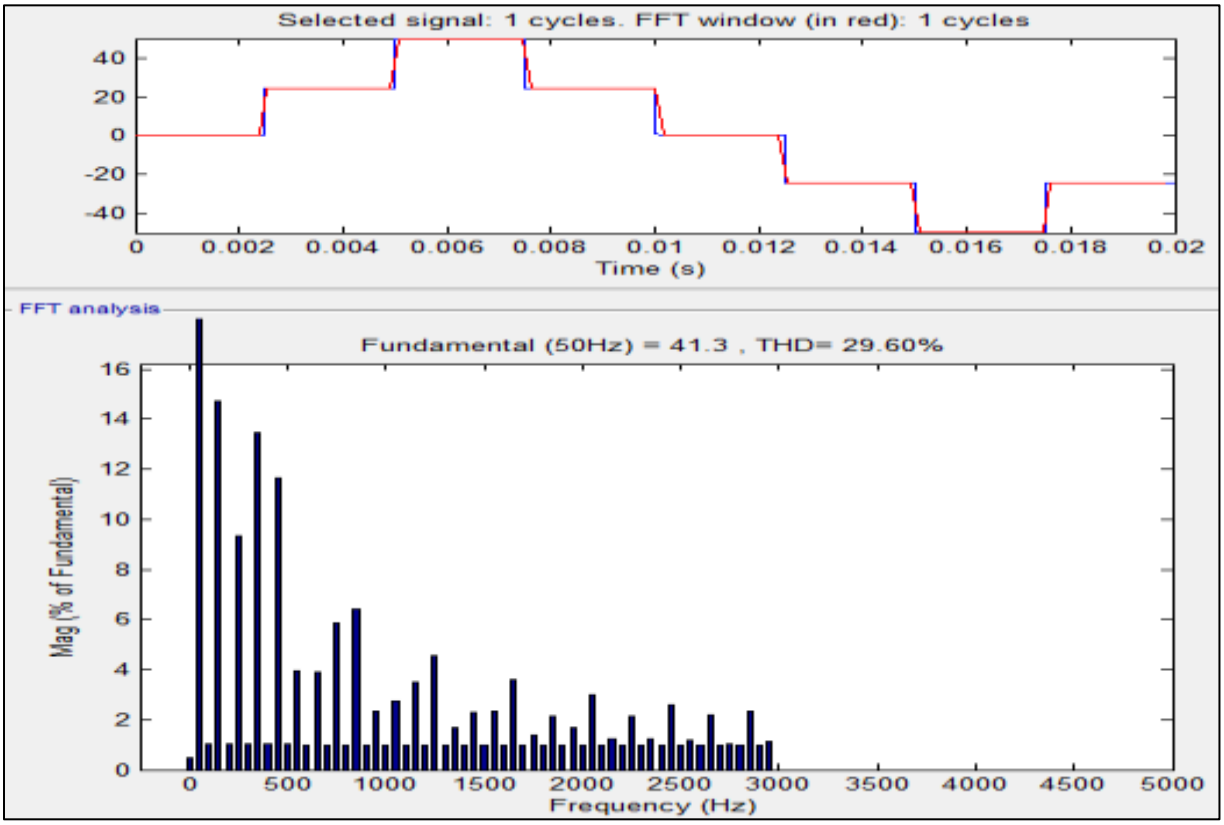

Fig. 3.4: Total harmonic distortion of five level DCMI

C. *Seven level diode clamped multilevel inverter*

Fig 3.5 shows the switching time and angle to generate triggering pulses (P1 to P12) for IGBT switches (S1 to S12) of seven level diode clamped multilevel inverter. The multi output voltages for the DC bus voltage of 100 V are 0V, 16.6V, 25V, 50V, -15.5V, -25V, -50V. To generate these multi voltages at the output of the Inverter, the time and pulse width of the pulse generators are arranged according to the switching time table shown in Fig 3.5.

Voltage Levels	0	Vdc/6 (16.6)	Vdc/4 (25)	Vdc/2 (50)	Vdc/4 (25)	Vdc/6 (16.6)	0	-Vdc/6 (-16.6)	- Vdc/4 (-25)	-Vdc/2 (-50)	-Vdc/4 (-25)	-Vdc/6 (-16.6)
Time(sec.)	0.0016	0.0033	0.005	0.0066	0.0083	0.01	0.0116	0.0133	0.015	0.0166	0.0183	0.02
Angle(Deg.)	30°	60°	90°	120°	150°	180°	210°	240°	270°	300°	330°	360°
P1				8.33%								
P2			PULSE	WIDTH	25%							
P3		PULSE	WIDTH	41.6%								
P4	PULSE	WIDTH	58.3%									
P5	PULSE	WIDTH	75%									
P6	PULSE	WIDTH	91.6%									
P7									PULSE	WIDTH	91.6%	
P8								PULSE	WIDTH	75%		
P9							PULSE	WIDTH	58.3%			
P10						PULSE	WIDTH	41.6%				
P11					PULSE	WIDTH	25%					
P12										8.33%		

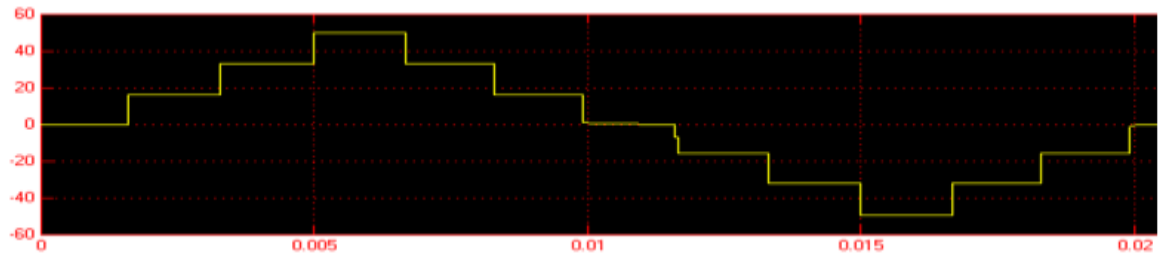

Fig. 3.5: Switching time table and output waveform of seven level DCMI

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Fig 3.6 shows the total harmonic distortion in the output voltage of seven level DCMI for the fundamental frequency of 50 Hz and Maximum frequency of 5000 Hz. The total harmonic distortion of 5-level DCMI was computed as 22.71%.

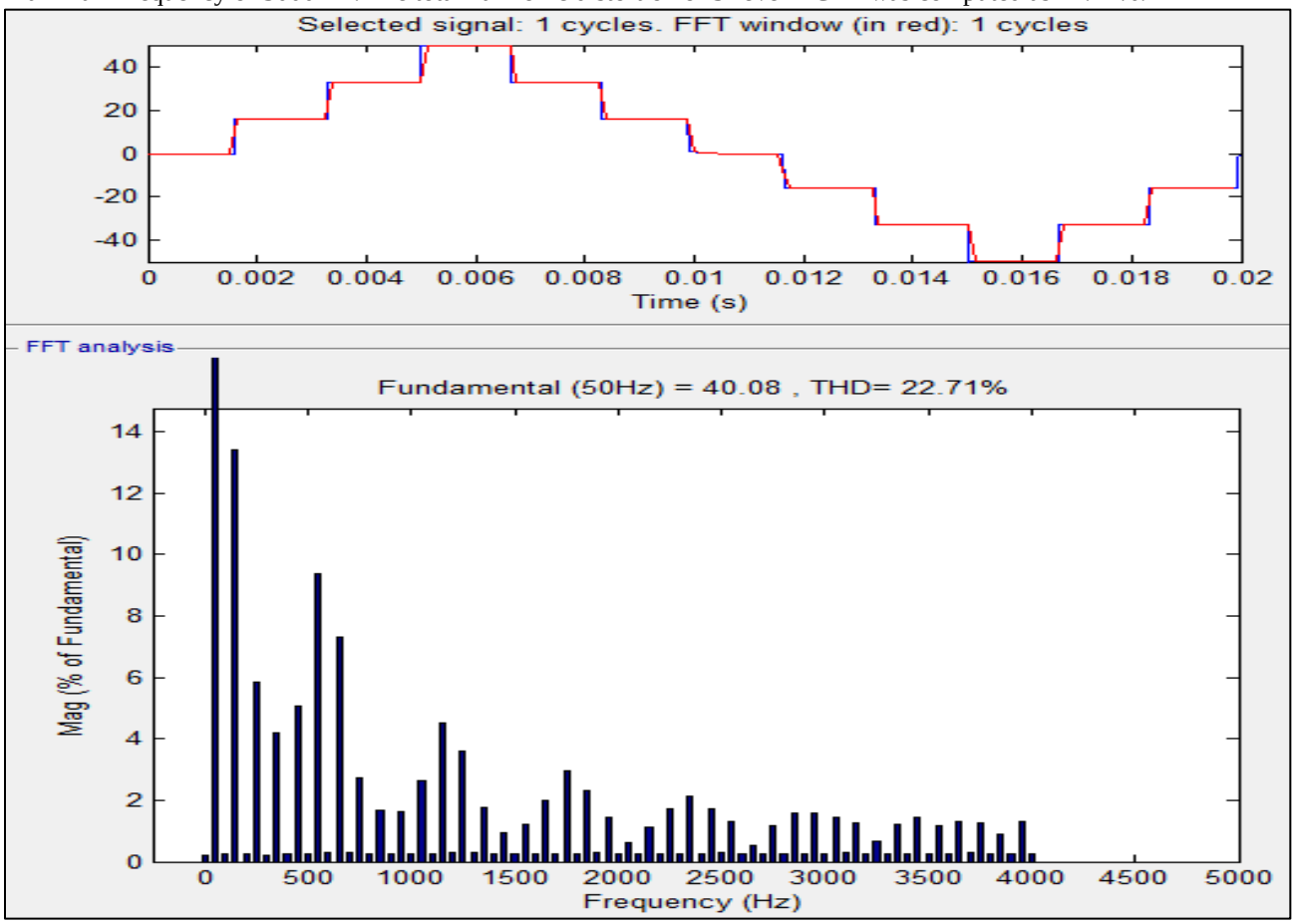

Fig. 3.6: Total harmonic distortion of seven level DCMI

IV. CONCLUSION

From the above discussion and results it can be concluded that the switching time table gives the clear idea to generate the required switching pulses for the Diode clamped multilevel inverters and also observed that the total harmonic distortion (%THD) in the output voltage will get reduced as the level of the inverter increases.

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