Design of Low Swing and Multi Threshold Voltage based Low Power 12T SRAM Cell: A Review

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Abstract

This paper focuses on the design of a novel low power twelve transistor static random access memory (12T SRAM) cell. In the proposed structure two voltage sources are used, one connected with the bit line and the other one connected with the bit-bar line in order to reduce the swing voltage at the output nodes of the bit and the bit-bar lines, respectively. Reduction in swing voltage reduces the dynamic power dissipation when the SRAM cell is in working mode. Low threshold voltage (LVT) transmission gate (TG) and two high threshold voltage (HVT) sleep transistors are used for applying the charge recycling technique. Stability of the proposed SRAM has also improved due to the reduction in swing voltage. Simulation results of power dissipation, access time, current leakage, stability and power delay product of the proposed SRAM cell have been determined and compared with those of some other existing models of SRAM cell. Simulation has been done in 45 nm CMOS environment. Tanner Tool is used for schematic design and layout design purpose.

Keywords: Charge Sharing, Leakage Low Power, Static Noise Margin, SRAM Swing Voltage

I. INTRODUCTION

The demand of battery operated high speed portable devices like notebook, laptop computers, personal digital assistants, cellular phones, etc. increase day by day. High speed portable devices require primary memory that responds faster. For that purpose, static random access memory (SRAM) is used, which is faster and refreshing is not needed again and again. Dynamic power dissipation and leakage current are the main issues of high speed SRAM cells because this unwanted power dissipation reduces the battery backup life of portable devices. A low power multiport SRAM with cross point write word lines shared write bit lines and shared write row access transistors approach has been shown. The design has one write, one read and two write, two read multiport SRAMs for register file applications in nano-scale CMOS technology. The cell features a cross point write word line structure to mitigate write half select disturb and improves the static noise margin (SNM). The write bit lines (WBLs) and write row access transistors are shared with adjacent bit cells to reduce the cell transistor count and area. The scheme halves the number of WBL, thus reducing WBL leakage and power consumption. So it is required to have a SRAM cell design, having both low static and dynamic power dissipations This approach is based on static power dissipation. In this present work a novel low power 12T SRAM cell is proposed. A charge recycling technique is used to minimize the leakage currents and static power dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. The different performance parameters have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells.

A. Proposed 12T SRAM cell

In order to overcome the problem associated with conventional SRAM cells and other existing SRAM cells, the authors proposes a multi threshold complementary metal oxide semiconductor (MTCMOS) based 12T SRAM architecture to achieve low static and dynamic power dissipations for read and write operations and better stability. In the proposed design two voltage sources V1 and V2 are connected to the outputs of the bit line (BL) and bitbar line respectively. Two NMOS transistors VT1 and VT2 are used, one connected with the BL and the other with the BL directly to switch ON and switch OFF the voltage sources during write operations. The voltage sources reduce the swing voltage during write '0' and write '1' operation at higher frequencies. This reduction in swing voltage reduces the dynamic power dissipation. The two high threshold voltage (HVT) sleep transistors S1 and S2 are used. NMOS sleep transistor S1 connects node M (also called virtual ground node) to ground whereas the PMOS sleep transistor S2, connects node N (also called the virtual supply node) to V_{dd} supply. The low threshold voltage (LVT) transmission gate (TG) is connected between the two virtual nodes M and N for providing charge sharing. The proposed design is illustrated Sleep transistor control signal (ST) and charge sharing control signal (CS) provide the switching activity control on sleep transistors and transmission gate, respectively. Sleep transistors disconnect logic cells from the supply and/or ground.

Charge recycling technique reduces the leakage current while transistors flip its mode from active to sleep and sleep to active. Reduction of leakage current reduces the static power dissipation.

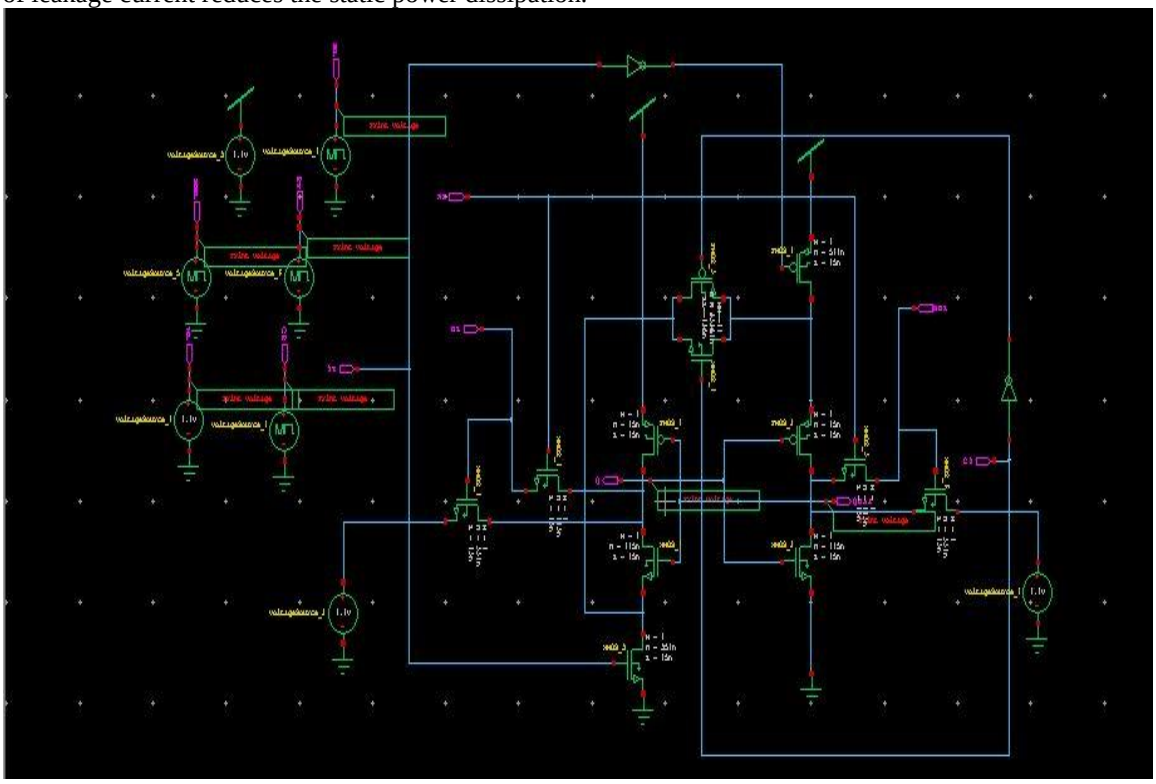

Fig. 1: The proposed 12T SRAM cell.

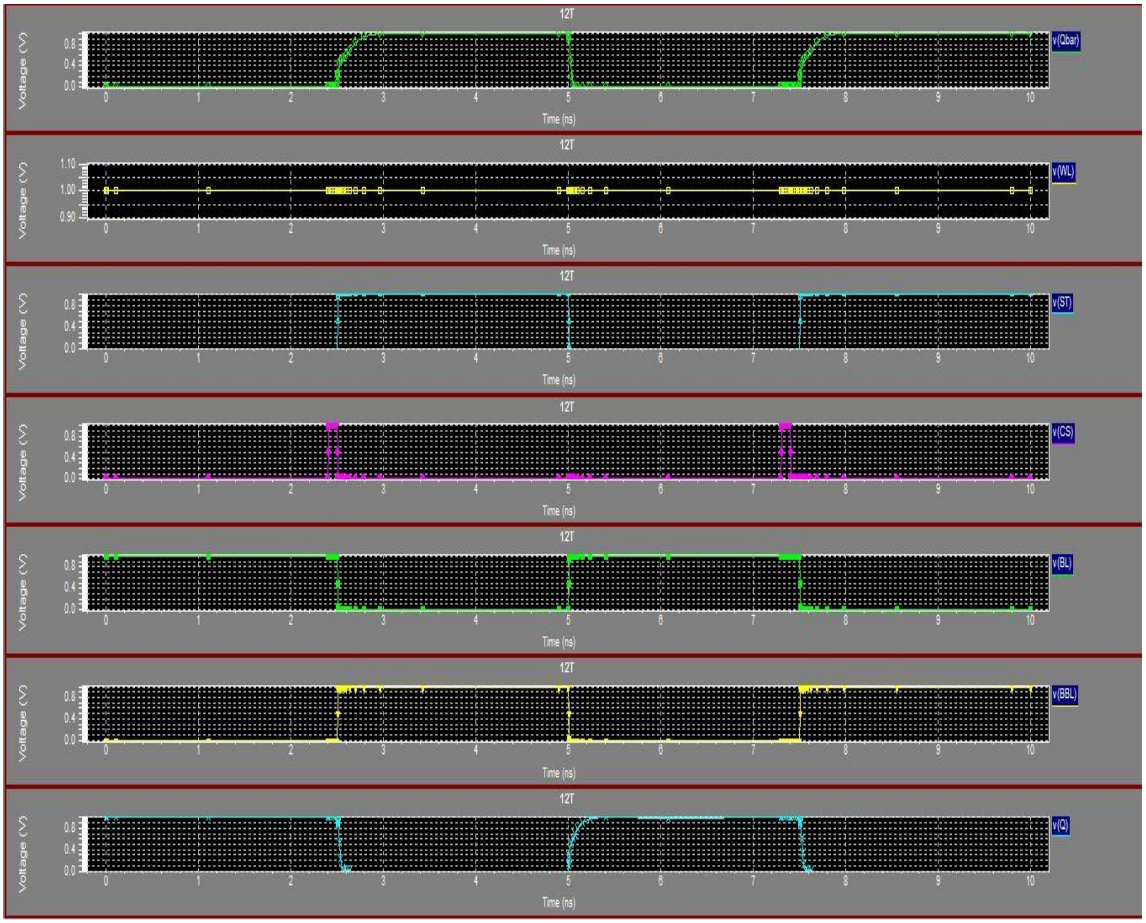

Fig. 2: Simulation Diagram of the proposed 12T SRAM cell.

II. RESULT AND CONCLUSION

Table – 1
Result & Conclusion

Parameters	*Based Paper 12T SRAM Cell*
Technology	*45nm*
Applied Voltage	*1v*
Power dissipation	*2.895uw*
Access time	*9.109ns*
Power delay product	*0.6371aJ*

The proposed SRAM cell also dissipates less static power during mode transitions due to charge recycling. Low leakage currents and the voltage sources provide better stability. Simulation has been done for power dissipations, static noise margin, access time, leakage current and power delay product for the proposed 12T SRAM cell and the results of the proposed SRAM cell are compared with those of other reported existing cells. The simulation shows that the proposed SRAM cell dissipates lesser dynamic power; has better stability; dissipates lesser current leakage during the mode transitions than the other existing SRAM cells.

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