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Design and Simulation of a Novel 8T SRAM Cell for Low Power High Speed Applications

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Abstract

Recently, the demand for portable communications has led to more and lower power ASIC (Application Specific Integrated Circuit) designs. It has been shown that power consumed during memory accesses accounts for a significant portion of the total power consumption in microprocessors, thus minimization of memory was as an important area of concern for today's IC designers. A new design contain transmission gate as an access transistor .Simulation results of power dissipation, access time, current leakage, stability and power delay product of the proposed SRAM cell have been determined and compared with those of some other existing models of SRAM cell.

Keywords: SRAM, Low Power VLSI, ASIC, Power Delay Product

I. INTRODUCTION

Depending on the type of load used at the inverter of Flip-Flop, the SRAM Cells are classified into three categories such as 4-Transistor cells, 6-Transistor cell and Thin-Film-Transistor (TFT) cell. Out of these three types 6-Transistor SRAM is widely used. SRAM cells stored the data as long as power supply is given, and it lost its stored data once power supply is removed. It doesn't require any periodic refreshment operation like DRAM because in SRAM data is stored in Flip-flop rather than in a capacitor. The data storage Static Random Access Memory cell contains a latch circuit which is usually stores the data of one bit and the memory cell contains two stable points at nodes A and B as shown in figure 1

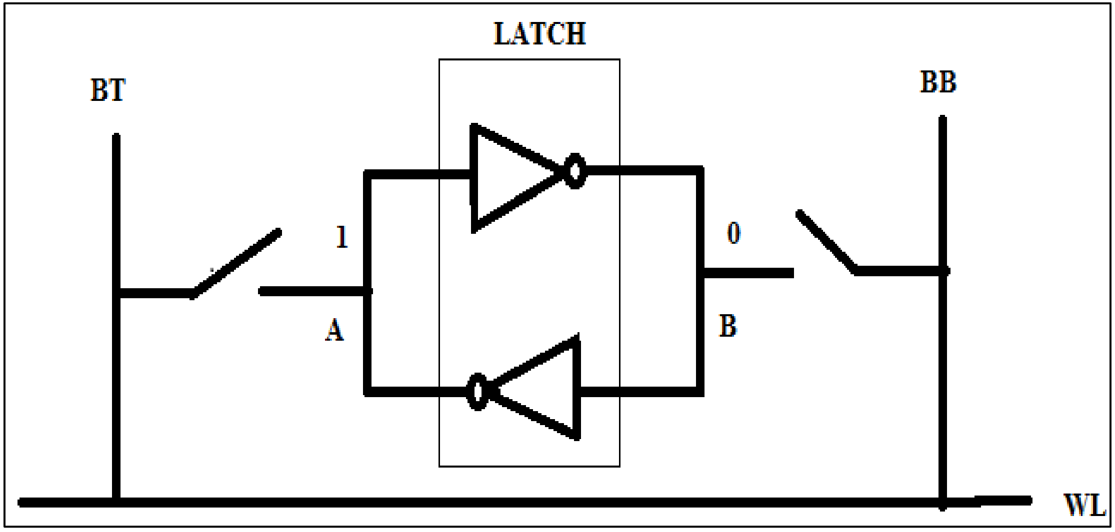

Fig. 1: Basic SRAM cell

Word line is used to access the data stored in the memory cell via complementary bit lines. Complementary data is stored at two bit lines which will enhance the performance of memory with respect to noise immunity and speed of operation

II. TRANSMISSION GATE

In principle, a transmission gate made up of two field-effect transistors, in which - in contrast to traditional discrete field effect transistors - the substrate terminal (Bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal.

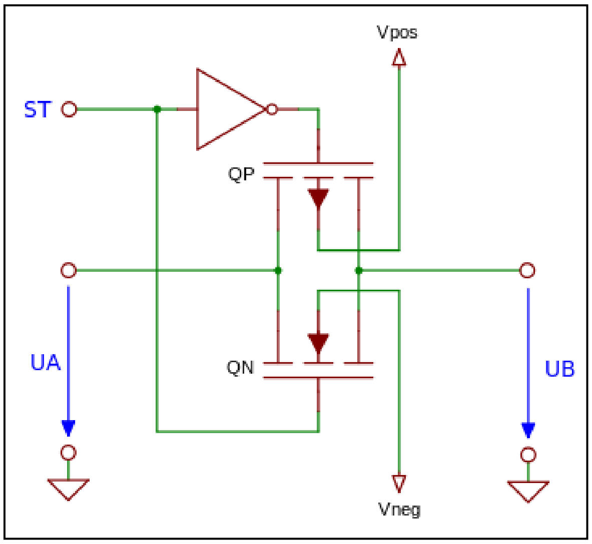

Fig. 2: Principle diagram of a transmission gate

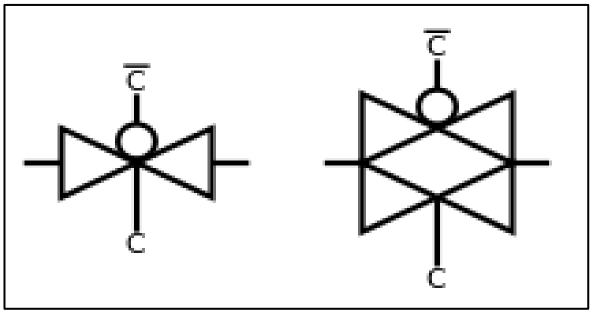

Fig. 3: Two variants of the "bow tie" symbol commonly used to represent a transmission gate

Two variants of the "bow tie" symbol commonly used to represent a transmission gate in circuit diagrams. Unlike with discrete FET transistors, the substrate terminal is not connected to the source connection. Instead, the substrate terminals are connected to the respective supply voltage potential in order to ensure that the parasitic substrate diode (between gate and substrate) is always reverse biased and so does not affect signal flow. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply voltage potential and the substrate terminal of the n-channel MOSFET connected to the negative supply voltage potential.

III. FUNCTION OF TRANSMISSION GATE

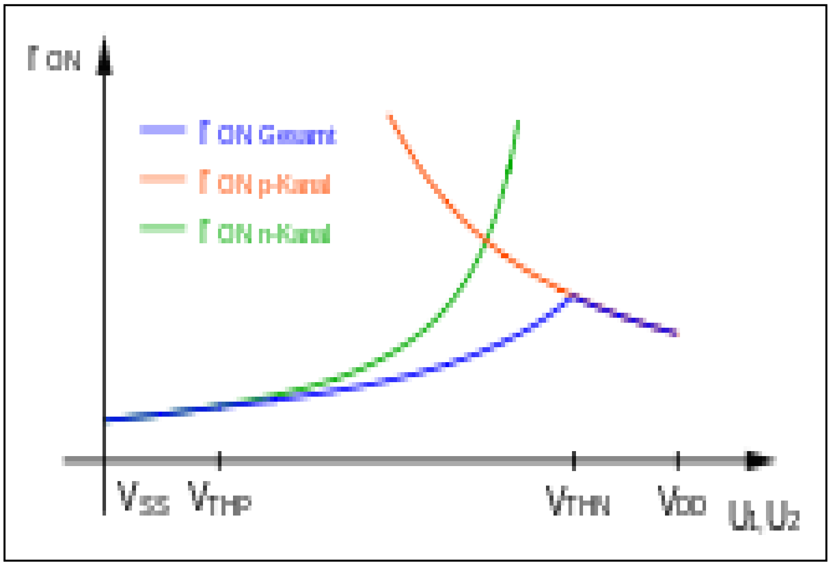

Fig. 4: Resistance characteristic of a transmission gate.

Resistance characteristic of a transmission gate. VTHN and VTHP denote those positions at which the voltage to be switched has reached a potential, where the threshold voltage of the respective transistor is reached. When the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off. When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts. One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the n-channel MOSFET, and this begins to turn off.

At the same time, the p-channel MOSFET has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches. Thereby it is achieved that the transmission gate passes over the entire voltage range. The transition resistance of the transmission gate varies depending upon the voltage to be switched, and corresponds to a superposition of the resistance curves of the two transistors. two transistors will conduct and the transmission gate turns off. When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts. One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET.

IV. PROPOSED 8T SRAM CELL

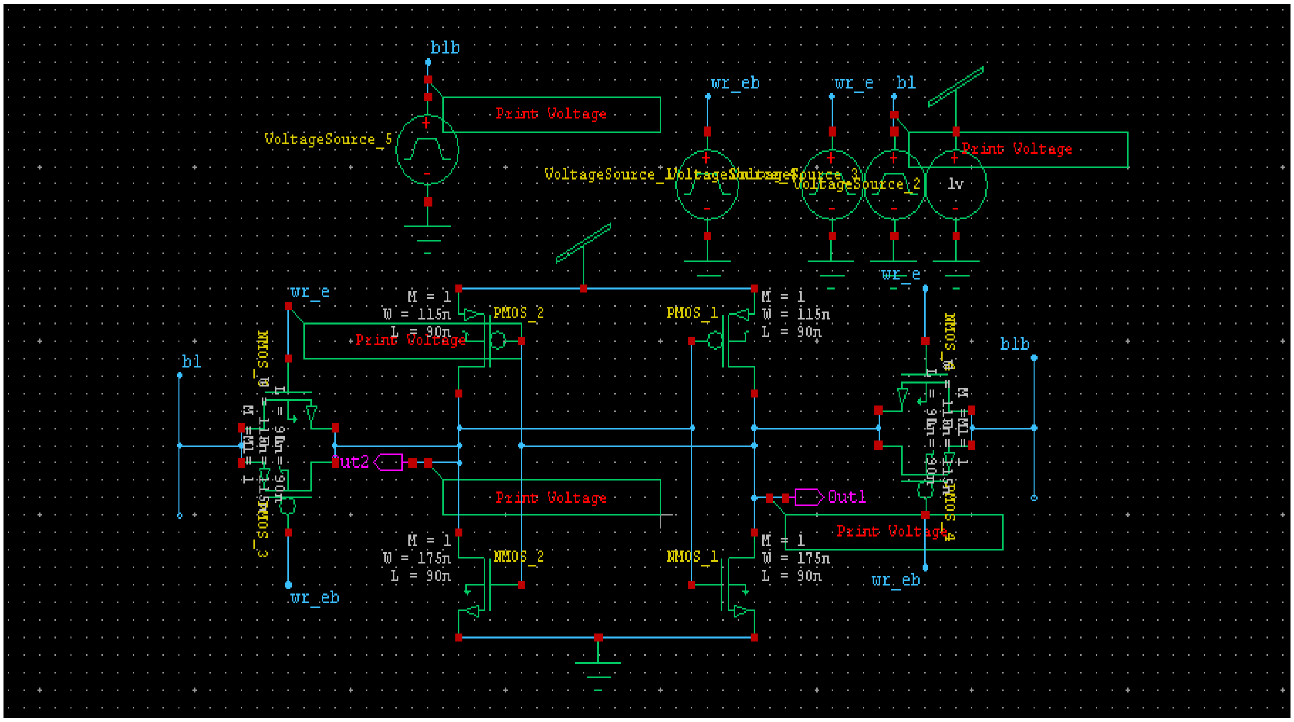

Fig. 5: Proposed 8T SRAM cell

Fig.5 shows circuit diagram of new proposed 12T SRAM cell working of proposed design is same as that of previous 8TSRAM cell but here we made some modification such as, in modification, what we have done is we have removed the voltage source used, so number of components reduced. We have placed TG in place of NMOS of both the access transistors; this will ensure true levels of output as we already know the advantage of TG over MOS. And we can see the effect of these modifications in our results, which are in next section.

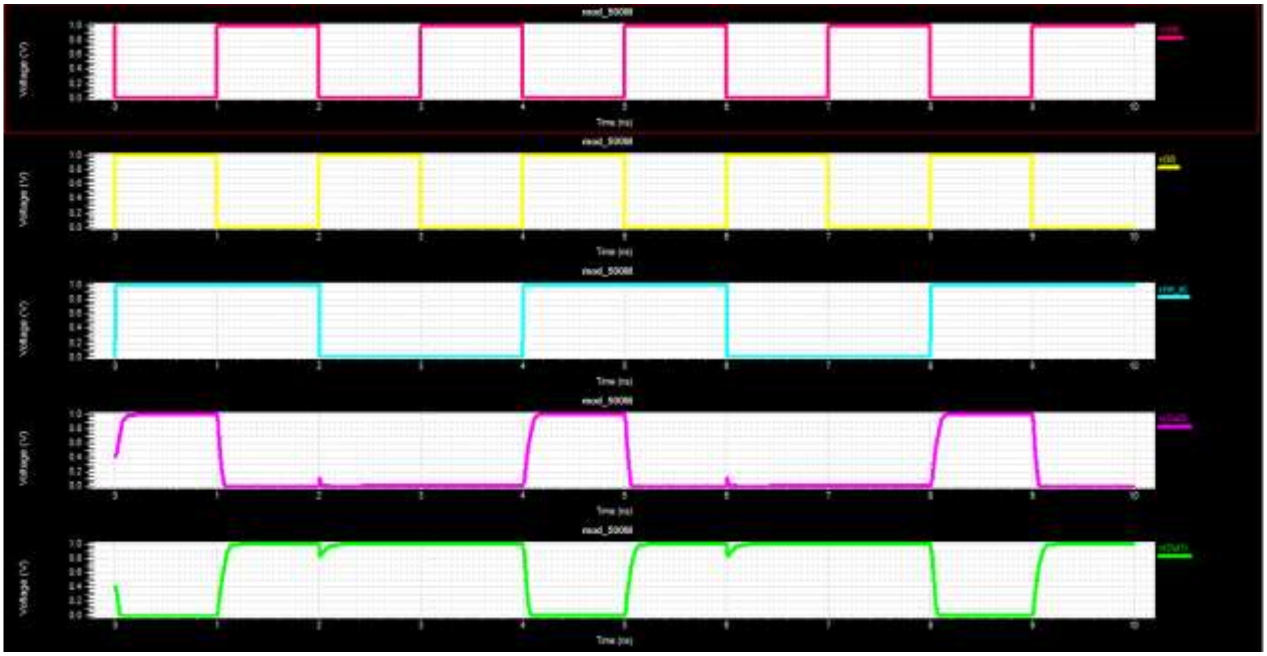

Fig. 6: Simulation Results of Proposed 8T SRAM Cell

A proposed design is simulated using Tanner EDA Tool using TSMC 90nm technology at 1V supply fig.6 shows output waveform of proposed 8TSRAM cell. Obtained result of new design is compared with old 8T SRAM cell and tabulated in table 1 as shown.

Table – 1
8T SRAM v/s Proposed 8T SRAM CELL Comparison

Frequency (in HZ)	*Power (in µW)*	*Write_1*		*Write_0*	
		Delay (ps)	*PDP (in a)*	*Delay (ps)*	*PDP (in a)*
Base Designs					
500M	*2.5731*	*74.940*	*192.828*	*45.319*	*116.610*
1G	*4.8162*	*73.133*	*352.223*	*45.552*	*219.387*
2G	*9.5662*	*73.084*	*699.136*	*45.542*	*435.663*
Modified Designs					
500M	*0.6065*	*46.744*	*28.350*	*28.349*	*17.193*
1G	*1.1601*	*47.548*	*55.160*	*27.739*	*32.180*
2G	*6.7268*	*69.041*	*464.442*	*33.972*	*228.522*

V. CONCLUSION

As, technology changes day by day power dissipation and stability are major issue of any high speed device. The proposed SRAM cell is solution of this problem which uses transmission gate as access transistor to give less power dissipation with high speed operation. A proposed novel 8T SRAM cell gives high speed and less power than previous design. Such high speed SRAM cell can be used in memory architecture such as flash memory. Simulation is carried using Tanner Tolls on TSMC 90nm technology.

VI. FUTURE SCOPE

Proposed SRAM cell gives very less power dissipation and high noise margin which is used in the memory design purpose. By selecting sense amplifier row decoder, recharge circuit SRAM memory can be design. The future works that can be conducted for manufacturing of 1MB chip using designed 2-kb block. For that 1MB memory need to design and draw a layout of the same using 2-kb block so that operating frequency will be near to 800MHz. All the post layout checks need to be done like antenna effect, EM check, electrostatic discharge, IR drop and need to check the reliability issues.

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