A Multi Threshold Technique Based 12T SRAM Cell for High Stability and Low Power Dissipation

Diwakar Prasad Tiwari
M. Tech Student
Department of Electronics & Communication Engineering
India IES College of Technology, Bhopal, India

Ashish Raghuwanshi
Assistant Professor
Department of Electronics & Communication Engineering
India IES College of Technology, Bhopal, India

Abstract

Framework on chip gadgets request segment which devour less power and gives less deferral in circuit. Versatile processors utilize memory component as a noteworthy part in their chip. This paper shows SRAM with transmission entryway rationale which gives less postponement and woks under low power supply. New SRAM configuration gives 0.40* lessening in power1.Also this SRAM cell gives 15*,0.90* change in write 0 and write1 than regular/conventional 12-T SRAM cell Tanner Tool is utilized for schematic outline and format configuration reason.

Keywords: Transmission Gate, Leakage Low power, Static noise margin, SRAM Swing Voltage, Tanner tool

I. INTRODUCTION

Decline in channel length requests a circuit which expend less power and less postponement. Fast convenient gadget, for example, portable, tablet, cpu requests rapid memory which devour less power and gives high signal to noise ratio. Smash memory is vital piece of any capacity hardware. Dynamic power dissemination and spillage/lekage current are the primary issues of fast SRAM cells since this undesirable power scattering lessens the battery reinforcement life of convenient gadgets. So it is required to have a SRAM cell configuration, having both low static and dynamic power dispersals.

In this present work a novel low power 12T SRAM cell is proposed. A charge reusing, in other words charge recycling method is utilized to limit the spillage streams i.e. leakage currents and static power dispersal amid the mode advances. Two voltage sources are utilized at the yield hubs to decrease the swing voltages, bringing about lessening of dynamic power dispersal amid exchanging movement. The diverse execution parameters have been resolved for the proposed SRAM cell and contrasted and those of the other existing SRAM cells.

The paper is organized as follows: Section 2 discusses about some existing SRAM cells, Section 3 describes circuit design and working principle of the proposed novel 12T SRAM cell. Section 4 describes the detailed analysis of the characteristics of the proposed cell and comparison with other existing SRAM cells and finally, Section 5 concludes the paper.

II. PROPOSED 12T SRAM CELL

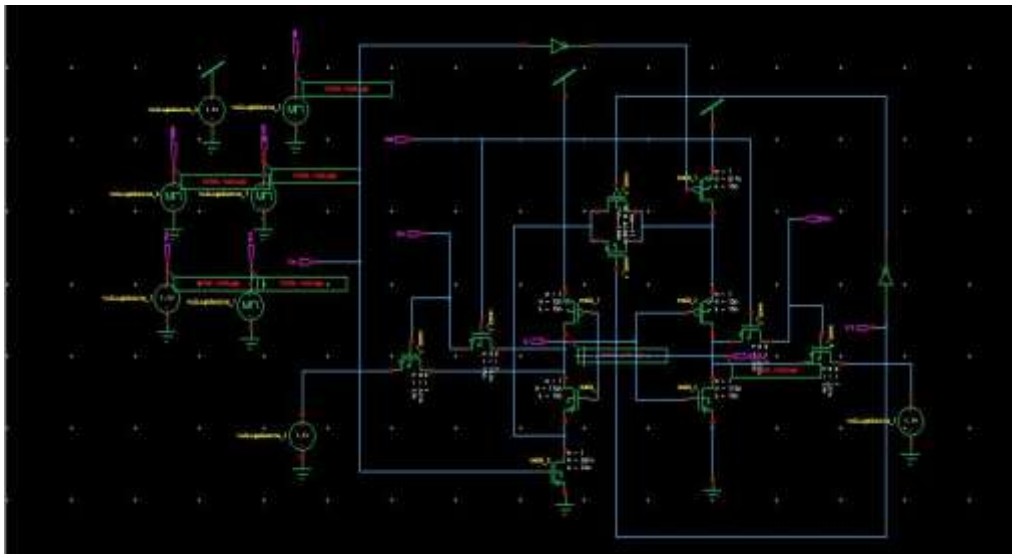

Fig. 1: The 12T SRAM cell.

In order to overcome the problem associated with conventional SRAM cells and other existing SRAM cells, the authors proposes a multi threshold complementary metal oxide semiconductor (MTCMOS) based 12T SRAM architecture to achieve low static and dynamic power dissipations for read and write operations and better stability. In the proposed design two voltage sources V1 and V2 are connected to the outputs of the bit line (BL) and bitbar line respectively. Two NMOS transistors VT1 and VT2 are used, one connected with the BL and the other with the BL directly to switch ON and switch OFF the voltage sources during write operations. The voltage sources reduce the swing voltage during write '0' and write '1' operation at higher frequencies. This reduction in swing voltage reduces the dynamic power dissipation. The two high threshold voltage (HVT) sleep transistors S1 and S2 are used. NMOS sleep transistor S1 connects node M (also called virtual ground node) to ground whereas the PMOS sleep transistor S2, connects node N (also called the virtual supply node) to Vdd supply. The low threshold voltage (LVT) transmission gate (TG) is connected between the two virtual nodes M and N for providing charge sharing. The proposed design is illustrated Sleep transistor control signal (ST) and charge sharing control signal (CS) provide the switching activity control on sleep transistors and transmission gate, respectively. Sleep transistors disconnect logic cells from the supply and/or ground. Charge recycling technique reduces the leakage current while transistors flip its mode from active to sleep and sleep to active. Reduction of leakage current reduces the static power dissipation.

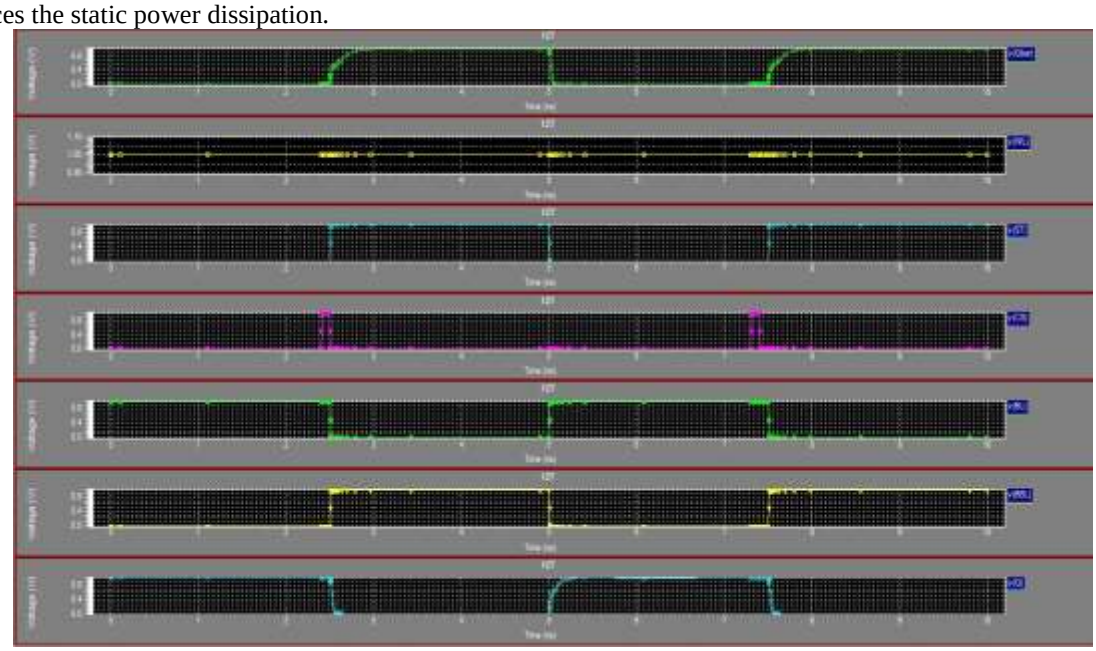

Fig. 2: Simulation Diagram of the 12T SRAM cell.

III. PROPOSED 12T SRAM CELL

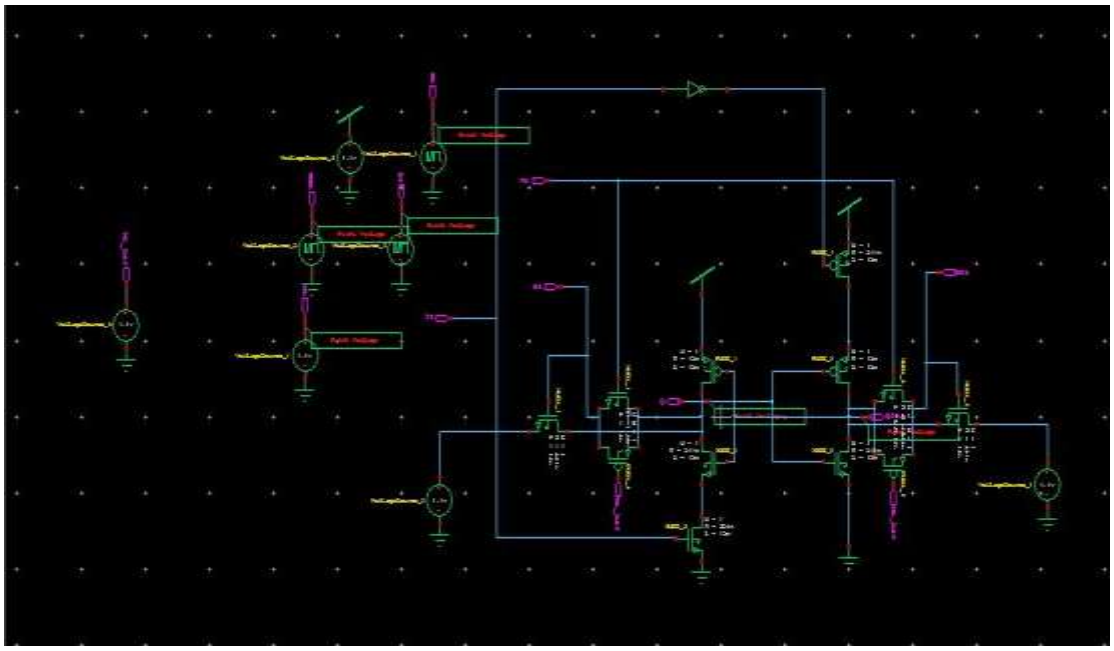

Fig. 3: The proposed 12T SRAM cell.

Fig.3 shows circuit diagram of new proposed 12T SRAM cell working of proposed design is same as that of previous 12TSRAM cell but here we made some modification such as, In modification, what we have done is We have removed the charge sharing block i.e. TG(Transmission Gate) structure and inverter used, so number of transistors reduced. We have placed TG in place of NMOS of both the access transistors, this will ensure true levels of output as we already know the advantage of TG over MOS. And we can see the effect of these modifications in our results, which are in next section.

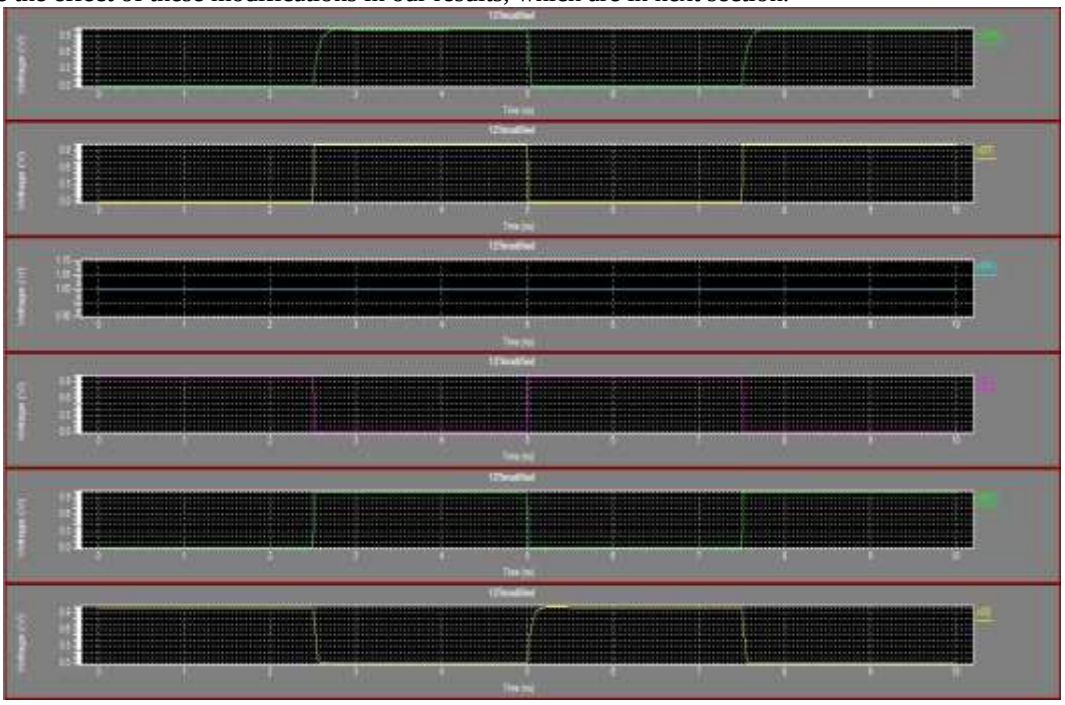

Fig. 4: Simulation Diagram of the proposed 12T SRAM cell.

IV. RESULT AND CONCLUSION

A proposed design is simulated using Tanner EDA Tool using TSMC 45nm technology at 1V supply.fig.4 shows output waveform of proposed 12TSRAM cell. Obtained result of new design is compared with old 12T SRAM cell and tabulated in table 1 as shown.

Table – 1
12T SRAM vs proposed 12T SRAM cell Comparison

Designs	*Power*	*Write 0*		*Write 1*		*SNM*
		Delay	*PDP*	*Delay*	*PDP*	
12T SRAM	*1.9844 uW*	*21.054 ps*	*41.780 aJ*	*22.995 ps*	*45.632 aJ*	*89mV*
Proposed 12T SRAM	*0.8000 uW*	*24.227 ps*	*19.384 aJ*	*20.921 ps*	*16.738 aJ*	*160mV*

V. CONCLUSION

A proposed novel 12T SRAM cell gives high signal to noise ratio than past outline. Such rapid, high SNM, SRAM cell can be utilized as a part of memory design, for example, streak/flash memory. As, innovation changes step by step control scattering and security are real issue of any fast gadget. The proposed SRAM cell is arrangement of this issue which utilizes transmission entryway as access transistor to give less power dissemination with rapid operation. In addition, quick operation of this SRAM offers advantage to use in advanced flag preparing and digital signal processing. Recreation is conveyed utilizing Tanner Tools on TSMC 45nm innovation/technology.

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