

A Three-Phase Multilevel Inverter using Limited Power Electronic Components

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Abstract

In this paper, a three-phase five-level voltage-source inverter is introduced with a new configuration. The proposed inverter constitutes of a conventional three-phase two-level bridge with three bi-directional switches. A multi-level dc-link using constant dc voltage supply and cascaded half-bridge is associated (linked) in such a way that the proposed inverter gives us the required output voltage levels. For the purpose of increasing the number of voltage levels with optimized number of power electronic components, it is recommended to use different methods to determine the magnitudes of utilized dc voltages. The important frequency staircase modulation method is easily used to generate the suitable switching gate signals. Moreover, the model type of the advised configuration can be manufactured as the obtained hardware & simulation results ensures its feasibility of the configuration and the compatibility of the modulation technique is precisely noted.

Keywords: Bidirectional Switch, Fundamental Frequency Staircase Modulation, Multilevel Inverter

I. INTRODUCTION

MULTI-LEVEL inverters comprises of a group of switching devices and dc supply voltages, which produces output voltages with stepped waveforms. Multi-level technology has started with the three-level converter followed by numerous multi-level converter topologies. Many distinct topologies and wide variety of control methods have been developed in the recent literatures. The common multi-level inverter configurations are Cascaded Hybrid Bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitor (FC). The unbalanced voltage in the dc link of FC, the deviating voltage of Neutral Point voltage in NPC, and the huge number of separated dc supplies in CHB are considered the main problems of these topologies. Apart from these three main topologies, few other topologies were introduced. Recently, hybrid multistage & asymmetrical topologies are becoming one of the utmost interested research area. The hybrid multistage converters comprises of different multi-level configurations with unequal dc supply voltages, whereas, in asymmetrical topologies, the magnitudes of dc supply voltages are unequal. These topologies not only reduces the cost but also improves the reliability and decreases the size of the inverters, because of the use of minimum number of power electronic components, capacitors, and dc supplies. With such inverters, different modulation strategies and power electronic technologies are required.

On the other hand, in order to improve the performance of the conventional single phase and three-phase inverters, different topologies using different types of bi-directional switches have been advised. Comparing to the unidirectional one, bi-directional switch is able to conduct the current and withstand the voltage in both directions. Bi-directional switches with a suitable control technique can enhance the performance of the multi-level inverters in terms of reducing the number of semiconductor devices, optimizing the withstanding voltage and achieving the desired output voltage with higher levels. Based upon this technical background, this paper suggests a topology for a three-phase five-level multi-level inverter. As the number of insulated-gate driver circuits, switching devices are minimized, so the installation area and cost also reduces significantly. The magnitudes of the utilized dc supply voltages have been selected in a way that increases the number of voltage levels with an effective application of a fundamental frequency staircase modulation technique. Extended structure for N-level is also presented and compared with the conventional well-known multilevel inverters. Hardware & Simulation results are given and explained.

II. PROPOSED TOPOLOGY

The typical configuration of the proposed three-phase five-level multilevel inverter is shown in Fig. 1(a) and (b). Three bi-directional switches (S1–S6, Da1–Dc2), two switches, two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The main work of these bi-directional switches is to block the higher voltage and ease current flow to and from the mid-point (o). A multi-level dc link built by a single dc supply voltage with fixed magnitude of 4Vdc and Cascaded Hybrid Bridge having two unequal dc supply voltages of Vdc and 2Vdc are connected to (+, –, o) bridge terminals. Based upon the required number of output voltage levels, a number of Cascaded Hybrid Bridge cells are used. Since the proposed inverter is designed to

achieve five voltage levels, the power circuit of the Cascaded Hybrid Bridge makes use of two series cells having two unequal dc supply voltages.

In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels.

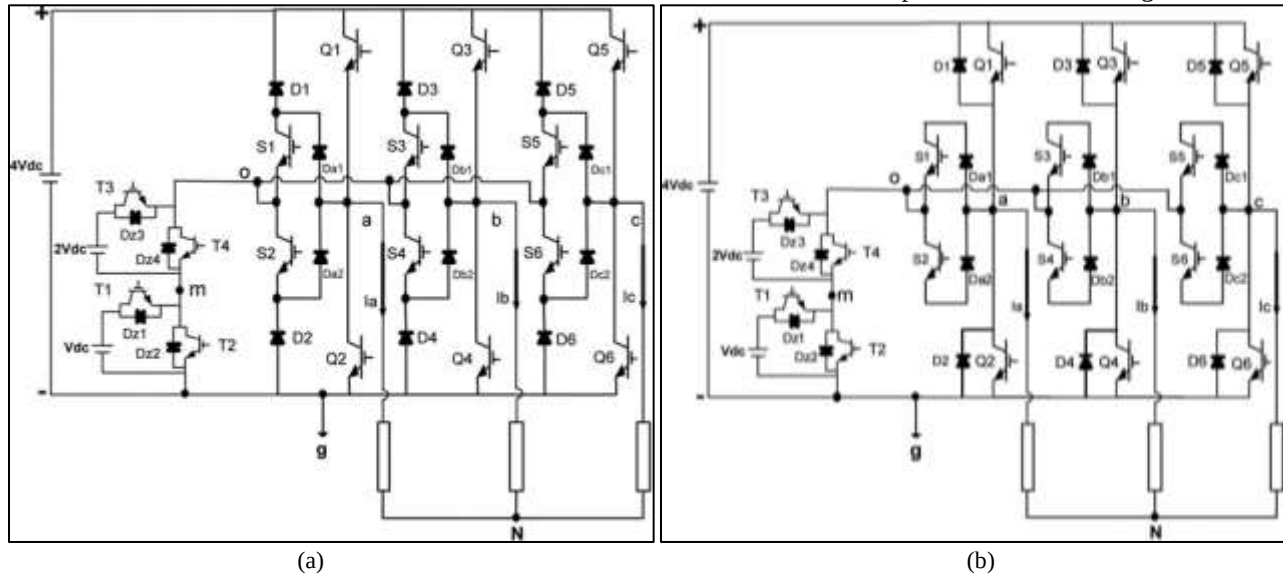


Fig. 1: Circuit Diagram of the Proposed Three-Phase Five-Level Multi-Level Inverter

A dc supply voltage V_{dc} of the first cell is added, if T1 (switch) is turned ON leading to $V_{mg} = +V_{dc}$, where V_{mg} means the voltage at node (m) with respect to inverter ground (g) or by-passed if T2 (switch) is turned ON leading to $V_{mg} = 0$.

Likewise, the dc supply voltage $2V_{dc}$ of the second cell is added when switch T3 is turned ON resulting in $V_{om} = +2V_{dc}$, where V_{om} is the voltage at mid-point (o) with respect to node (m) or bypassed when switch T4 is turned ON resulting in $V_{om} = 0$. The peak voltage rating of the switches of the conventional two-level bridge (Q1–Q6) is $4V_{dc}$ whereas the bidirectional switches (S1–S6) have a peak voltage rating of $3V_{dc}$. In CHB cells, the peak voltage rating of second cell switches (T3 and T4) is $2V_{dc}$ while the peak voltage rating of T1 and T2 in case of first cell is V_{dc} . By considering phase a, the operating status of the switches and the inverter line-to-ground voltage V_{ag} are given in Table 1.

Table - 1
Switching State S_a and Inverter Line-to-Ground Voltage V_{ag}

S_a	Q1	S1	S2	Q2	T1	T2	T3	T4	V_{ag}
4	on	off	off	off	on	off	on	off	$+4V_{dc}$
3	off	on	on	off	on	off	on	off	$+3V_{dc}$
2	off	on	on	off	off	on	on	off	$+2V_{dc}$
1	off	on	on	off	on	off	off	on	$+V_{dc}$
0	off	off	off	on	on	off	off	on	0

It is easier to express the inverter line-to-ground voltages V_{ag} , V_{bg} , and V_{cg} in terms of their switching states S_a , S_b , and S_c as

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \quad (1)$$

where $N = 5$ is the maximum number of voltage levels.

The balanced load voltages can be attained if the proposed inverter operates on the switching states represented in Table 2. Within a cycle of the output waveform, the inverter may have 24 different modes. According to Table 2, it can be observed that the bi-directional switches operate in 18 modes. For each mode, there is no more than one bi-directional switch in on-state. Because of which the load current commutates over one switch and one diode, the load current I_b will flow in S3 and Db1 or S4 and Db2). Since some insulated-gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed topology significantly contributed in dropping the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms V_{ab} , V_{bc} , and V_{ca} with corresponding switching gate signals are depicted in Fig. 2

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (2)$$

The inverter line-to-neutral voltages V_{aN} , V_{bN} , and V_{cN} may be expressed as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (3)$$

It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to the midpoint (o) are given by

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} - \begin{bmatrix} V_{og} \\ V_{og} \\ V_{og} \end{bmatrix} \quad (4)$$

where V_{og} is the voltage at midpoint (o) with respect to ground (g). V_{og} routinely fluctuates among three different voltage values V_{dc} , $2V_{dc}$, and $3V_{dc}$ as follows:

$$V_{og} = \begin{cases} V_{dc}, & \text{if } S_a + S_b + S_c \leq 5 \\ 2V_{dc} & \text{if } S_a + S_b + S_c = 6 \\ 3V_{dc} & \text{if } S_a + S_b + S_c \geq 7 \end{cases}$$

The simulated voltage waveforms of V_{ag} , V_{og} , V_{ao} , and V_{aN} based on (1)–(5) are shown in Fig. 3 where, for instance, 13

Table - 2

Switching States Sequence of the Proposed Inverter within One Cycle

$S_a S_b S_c$	Period T [s]	ON switches Leg a	ON switches Leg b	ON switches Leg c	ON switches cascaded half-bridge	V_{ag} [V]	V_{bg} [V]	V_{cg} [V]
400	t1	Q1	Q4	Q6	T1, T4	$4V_{dc}$	0	0
410	t2	Q1	S3, S4	Q6	T1, T4	$4V_{dc}$	V_{dc}	0
420	t3	Q1	S3, S4	Q6	T2, T3	$4V_{dc}$	$2V_{dc}$	0
430	t4	Q1	S3, S4	Q6	T1, T3	$4V_{dc}$	$3V_{dc}$	0
440	t5	Q1	Q3	Q6	T1, T3	$4V_{dc}$	$4V_{dc}$	0
340	t6	S1, S2	Q3	Q6	T1, T3	$3V_{dc}$	$4V_{dc}$	0
240	t7	S1, S2	Q3	Q6	T2, T3	$2V_{dc}$	$4V_{dc}$	0
140	t8	S1, S2	Q3	Q6	T1, T4	V_{dc}	$4V_{dc}$	0
040	t9	Q2	Q3	Q6	T1, T4	0	$4V_{dc}$	0
041	t10	Q2	Q3	S5, S6	T1, T4	0	$4V_{dc}$	V_{dc}
042	t11	Q2	Q3	S5, S6	T2, T3	0	$4V_{dc}$	$2V_{dc}$
043	t12	Q2	Q3	S5, S6	T1, T3	0	$4V_{dc}$	$3V_{dc}$
044	t13	Q2	Q3	Q5	T1, T3	0	$4V_{dc}$	$4V_{dc}$
034	t14	Q2	S3, S4	Q5	T1, T3	0	$3V_{dc}$	$4V_{dc}$
024	t15	Q2	S3, S4	Q5	T2, T3	0	$2V_{dc}$	$4V_{dc}$
014	t16	Q2	S3, S4	Q5	T1, T4	0	V_{dc}	$4V_{dc}$
004	t17	Q2	Q4	Q5	T1, T4	0	0	$4V_{dc}$
104	t18	S1, S2	Q4	Q5	T1, T4	V_{dc}	0	$4V_{dc}$
204	t19	S1, S2	Q4	Q5	T2, T3	$2V_{dc}$	0	$4V_{dc}$
304	t20	S1, S2	Q4	Q5	T1, T3	$3V_{dc}$	0	$4V_{dc}$
404	t21	Q1	Q4	Q5	T1, T3	$4V_{dc}$	0	$4V_{dc}$
403	t22	Q1	Q4	S5, S6	T1, T3	$4V_{dc}$	0	$3V_{dc}$
402	t23	Q1	Q4	S5, S6	T2, T3	$4V_{dc}$	0	$2V_{dc}$
401	t24	Q1	Q4	S5, S6	T1, T4	$4V_{dc}$	0	V_{dc}

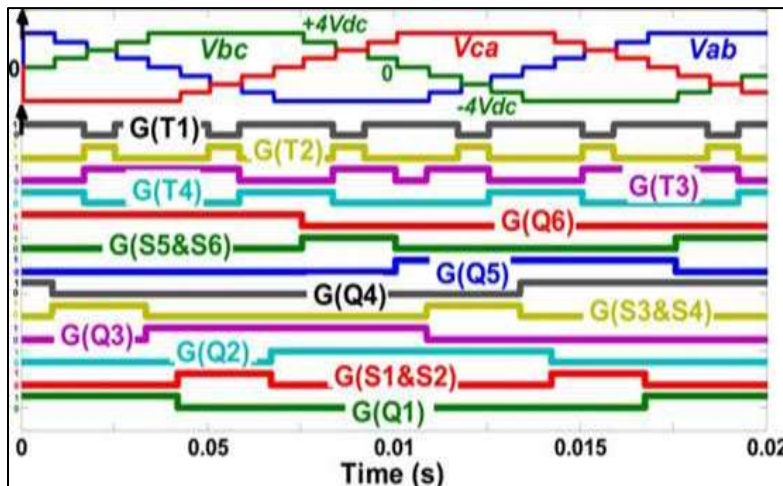


Fig. 2: Simulated waveforms of V_{ab} , V_{bc} , and V_{ca} with corresponding switching gate signals for the proposed inverter at fundamental frequency $f = 50$ Hz

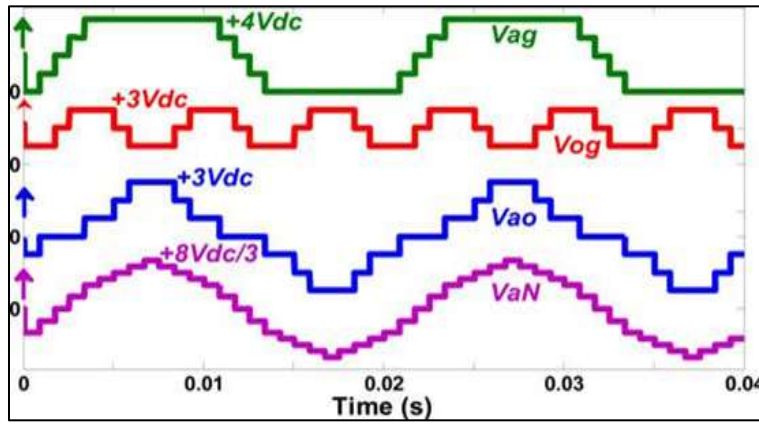


Fig. 3: Simulated waveforms of Vag, Vog, Vao, and Va N for the proposed inverter $f = 50$ Hz

The sequent voltage steps are seen in VaN waveform as follows: $+8V_{dc}/3$, $+7V_{dc}/3$, $+6V_{dc}/3$, $+5V_{dc}/3$, $+4V_{dc}/3$, $+2V_{dc}/3$, 0 , $-2V_{dc}/3$, $-4V_{dc}/3$, $-5V_{dc}/3$, $-6V_{dc}/3$, $-7V_{dc}/3$, and $-8V_{dc}/3$. It is worth noting that all simulated waveforms are obtained at $t_1 = t_2 = \dots = t_{24} = 0.02/24$ s. In order to plot the space vector diagram of the proposed inverter in a stationary d-q reference frame, the following equations can be used to derive d and q voltage components for all inverter vectors:

$$V_q = \frac{4V_{dc}}{3(N-1)}(2S_a - S_b - S_c) \quad (6)$$

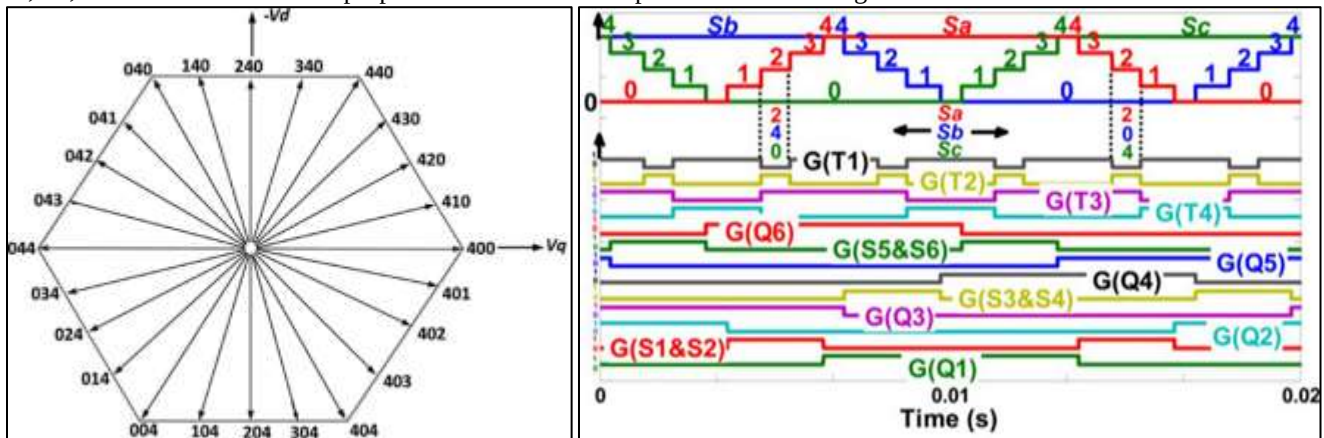
$$V_d = \frac{4V_{dc}}{\sqrt{3}(N-1)}(S_c - S_b) \quad (7)$$

$$V = V_q - jV_d \quad (8)$$

For all switching states presented in Table II, Fig. 4 shows the space vector diagram for the proposed topology.

III. SWITCHING ALGORITHM

For the proposed inverter, we can simply implement the staircase modulation. The most common modulation technique used to control the fundamental output voltage as well as to eliminate the unwanted harmonic components from the output waveforms is Staircase modulation with selective harmonic. The Newton-Raphson method is normally used to find out the solutions to $(N-1)$ non-linear transcendental equations. The problematic calculations and the need of high performance controller for the real time applications are the main disadvantages of such method. Hence, an alternative method is proposed to produce the inverter's switching gate signals. It is very easy to control the proposed inverter and achieve the required output voltage waveforms in terms of S_a , S_b , and S_c . The basis of the proposed method can be explained as succeeding:



Or a given value of modulation index M_a and within a full cycle of the operation of the proposed inverter, the switching states S_a , S_b , and S_c are determined instantly. The on-time calculations of S_a , S_b , and S_c directly depend on the instantaneous values of the inverter line-to-ground voltages. It is very well known that the reference values of V_{ag} , V_{bg} , and V_{cg} are normally given by

$$\begin{bmatrix} V_{ag_ref} \\ V_{bg_ref} \\ V_{cg_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) \end{bmatrix} + \frac{4V_{dc}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$

where wt is the electrical angle. Or

$$\begin{bmatrix} V_{ag_ref} \\ V_{bg_ref} \\ V_{cg_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) \end{bmatrix} + \frac{4V_{dc}}{2} * \left[1 - \frac{M_a}{6} \cos(3wt) \right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (10)$$

From (10), it can be observed that the third harmonic component is summed to the three-line-to-ground voltages. The third harmonic injection may rise the inverter fundamental voltage without causing over modulation. As a result, M_a can reach to 1.15 and S_a , S_b , and S_c can be simply determined by integerizing the reference line-to-ground voltages as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{integer} \left(\frac{N-1}{4V_{dc}} * \begin{bmatrix} V_{ag_ref} \\ V_{bg_ref} \\ V_{cg_ref} \end{bmatrix} \right) \quad (11)$$

The proposed modulation method is compared with the Stair case modulation with the selective harmonic method. The proposed modulation features needs less time and have simple calculations. The inverter's operating switching states S_a , S_b , & S_c and the corresponding switching gate signals based on the proposed modulation method are shown in Fig. 5. Fig. 5. Inverter's operating switching states S_a , S_b , & S_c with corresponding switching gate signals based on the proposed modulation method.

Table 3
Switching State S_a 1 & Inverter Line-To-Ground Voltage V_{ag} AT $M_a < 0.9$ (LEG a)

S_a	$Q1$	$S1$	$S2$	$Q2$	$T1$	$T2$	$T3$	$T4$	V_{ag}
2	On	off	off	off	off	On	On	off	$+4V_{dc}$
1	off	On	On	off	off	On	On	off	$+2V_{dc}$
0	off	off	off	On	off	On	On	off	0

It is clear that the switching gate signals are generated within 24 different modes starting from (044) to (034). Since the proposed converter has been designed in order to achieve 5 voltage levels, the modulation index must be within range $0.9 \leq M_a \leq 1.15$. For modulation index $M_a < 0.9$, only two dc voltage supplies $4V_{dc}$ and $2V_{dc}$ are employed and the behavior of the proposed inverter becomes similar to the three-level multi-level inverter. Using (9)–(11) and substituting $N = 3$, the inverter's operating switching states S_a , S_b , and S_c at $M_a < 0.9$ can be defined. The principle of operation of the proposed inverter at $M_a < 0.9$ is illustrated in Table 3. Fig. 6(a) and Fig. 6(b) shows the inverter line-to-line voltage waveforms at 5 different modulation indices including the over modulation operation $M_a = 0.8, 0.9, 1.05, 1.15$, and 1.3 .

IV. EXTENDED STRUCTURE

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multilevel inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. 7(a) and (b). In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies.

1) All cells have an equal dc supply in magnitude.

$$V_{dc1} = V_{dc2} = \dots = V_{dcn} = V_{dc} \quad (12)$$

Then, the magnitude of fixed dc supply can be chosen as

$$V_{fix} = (N-1)V_{dc} = (1+n)V_{dc} \quad (13)$$

where n is the number of utilized cells. The maximum number of voltage steps is related to the number of utilized cells by

$$N = n + 2 \quad (14)$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform can be expressed as

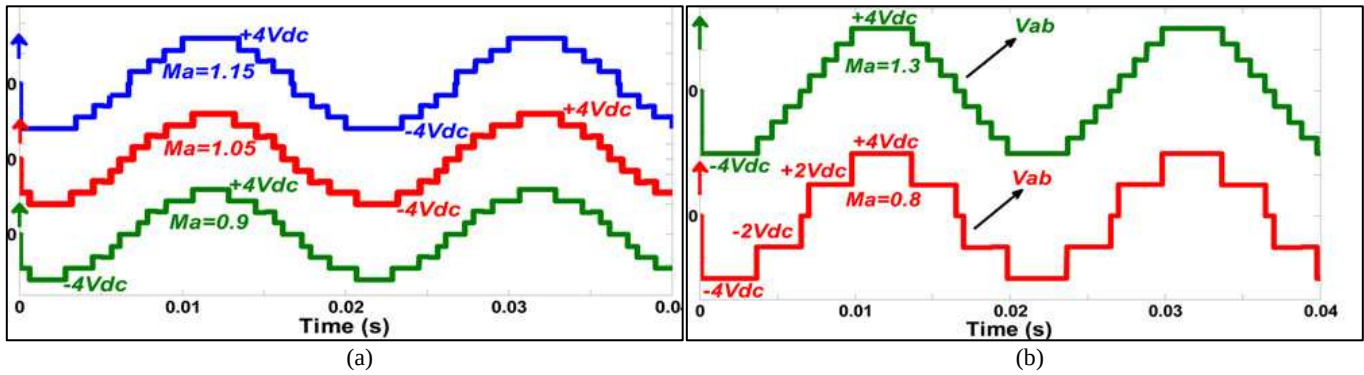


Fig. 6: Simulated waveforms of Vab at different modulation indices for the proposed inverter: (a) Ma = 0.9, 1.05, and 1.15 and (b) Ma = 0.8 and 1.3

$$M = 6(N - 1) \quad (15)$$

2) The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$V_{dc1} = V_{dc} \quad (16)$$

$$V_{dc2} = 2V_{dc} \quad (17)$$

$$V_{dcn} = nV_{dc} \quad (18)$$

$$V_{fix} = (N - 1)V_{dc} = \left[1 + \frac{n(n+1)}{2} \right] V_{dc} \quad (19)$$

$$N = 2 + \frac{n(n+1)}{2} \quad (20)$$

$$M = 6(N - 1) \quad (21)$$

3) By making a binary (power of 2) relationship between the dc supplies of the CHB structure as follows:

$$V_{dc1} = 2^{(0)}(V_{dc}) \quad (22)$$

$$V_{dc2} = 2^{(1)}(V_{dc}) \quad (23)$$

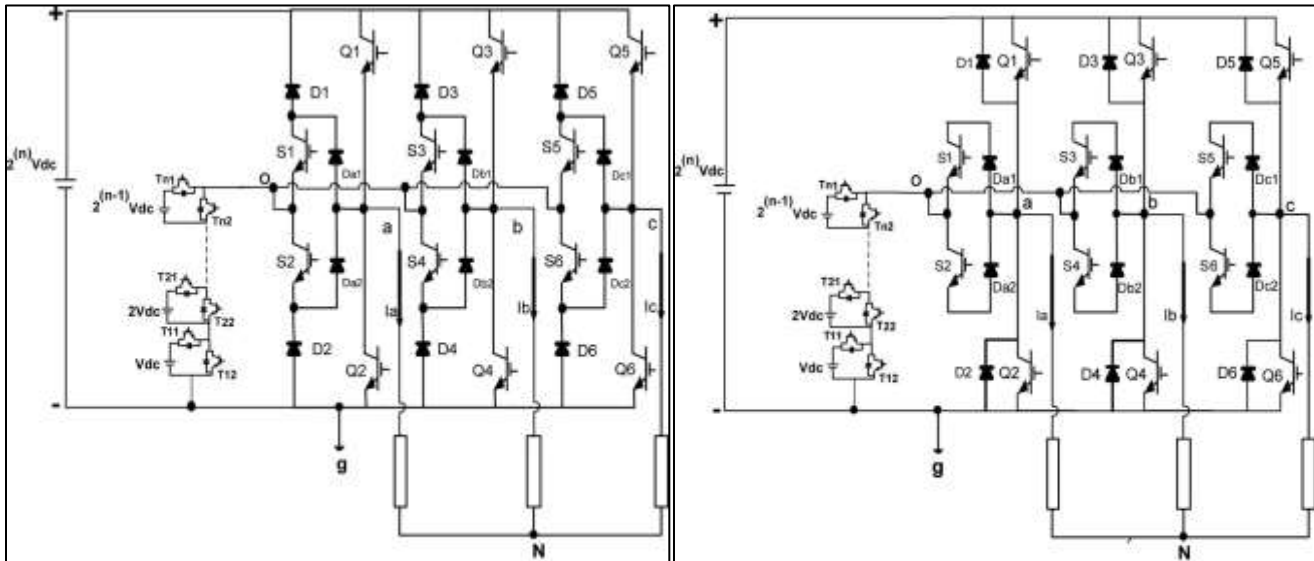


Fig. 7: Circuit Diagram of the Proposed Three-Phase N-Level Multi-Level Inverter (Third Method)

$$V_{dcn} = 2^{(n-1)}(V_{dc}) \quad (24)$$

$$V_{fix} = (N - 1)V_{dc} = \left[1 + \sum_{j=1}^n 2^{j-1} \right] V_{dc} = (2^n)V_{dc} \quad (25)$$

$$N = 1 + 2^n \quad (26)$$

$$M = 6(N - 1) \quad (27)$$

Table 4 illustrates some characteristics of the proposed methods.

Table - 4

Comparison of the Maximum Number of Voltage Levels with the Required Value of DC Voltage Supplies among the Proposed Methods

No of Cells	First Method			Second Method			Third Method		
	N	M	Vfix	N	M	Vfix	N	M	Vfix
2	4	18	3Vdc	5	24	4Vdc	5	24	4Vdc
3	5	24	4Vdc	8	42	7Vdc	9	48	8Vdc
4	6	30	5Vdc	12	66	11Vdc	17	96	16Vdc
5	7	36	6Vdc	17	96	16Vdc	33	192	32Vdc
6	8	42	7Vdc	23	132	22Vdc	65	384	64Vdc

Based upon the comparison carried among the various proposed methods, some observations are given below.

- 1) The first method as compared to the second and third methods, has a high modularity degree because of the symmetric structure of CHB makes use of equal dc voltage supplies. This method helps the proposed inverter to reach the maximum number of voltage levels (4, 5, 6, 7, 8, . . . ,N).
- 2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the necessary output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17, . . . with less number of dc supply voltages and power electronic components.

V. COMPARISON STUDY

In order to investigate the capability of the suggested topology, the proposed inverter is compared with different types of multi-level inverters such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and the Cascaded H-Bridge (CHB). It is obvious that the suggested three-phase N-level multi-level inverter can considerably reduce the required number of power electronic components. For the same number of output voltage levels ($N \geq 4$), Table 5 describes the required number of dc voltage supplies, control signals, switches, clamping diodes, and balancing capacitors of the proposed N-level inverter compared with the three existing inverters Neutral Point Clamped (NPC), Flying Capacitor (FC), and the Cascaded H-Bridge (CHB). As shown in Fig. 8, it can be observed that nearly more than two-third of number of switches can be counted out as N increases. For example, at the same number of voltage levels $N = 17$, and when compared with the existing multi-level inverters which require 96 switches, the required number of switches for the proposed inverter is comparatively less, since it requires 42 switches based on the first method, 22 switches based on the second method, and 20 switches based on the third method. On the other hand, it is well-known that the voltage and current ratings of the power electronic components have an effect on the cost and realization of the multi-level inverter. Assuming that all power components have an equal current rating which is the rated current of the load (I_L), the voltage ratings of these components depend on the magnitude of dc supply voltage, voltage stress, and structure of the inverter. Considering that all inverters have the same input dc link which equals $(N-1) V_{dc}$, Table 6 illustrates the rating requirements for the proposed inverter when compared with the rating requirements for the existing inverters. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are employed, the semiconductor devices expenses are considerably recovered.

VI. POWER CONVERSION EFFICIENCY & TOTAL HARMONIC DISTORTION (THD %)

In order to regulate the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the power electronics components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: Switching loss (P_{sw}) & conduction loss (P_{con}) as follows:

$$P_{sw_IGBT} = \frac{1}{T} \int_0^T E_{on}(t) dt + \frac{1}{T} \int_0^T E_{off}(t) dt \quad (28)$$

$$P_{sw_diode} = \frac{1}{T} \int_0^T E_{rr}(t) dt \quad (29)$$

Where $E_{on}(t)$ is a turn-on loss and $E_{off}(t)$ is a turn-off loss. Switching losses $E_{on}(t)$ and $E_{off}(t)$ are experienced during the ON and OFF states, respectively. While $E_{rr}(t)$ is the reverse recovery loss of the diode, the majority of switching loss, which is experienced when the diode is in OFF state.

$$P_{con_IGBT} = \frac{1}{T} \int_0^T V_{on_IGBT} i(t) dt \quad (30)$$

$$P_{con_Diode} = \frac{1}{T} \int_0^T V_{on_diode} i(t) dt \quad (31)$$

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops V_{on} IGBT, V_{on} diode, and the instantaneous current $i(t)$ flowing through IGBT or diode. The total losses P_t are expressed as follows:

$$P_t = P_{con} + P_{sw} \quad (32)$$

Once the total semiconductor losses P_t in the introduced inverter are defined, the relative inverter efficiency is determined based on the following expression:

$$n\% = \frac{P_{out}}{P_t + P_{out}} \times 100 \quad (33)$$

The probable current directions with corresponding conducting devices in phase are given in Table 7. A MATLAB/Simulink model of the proposed inverter shown in Fig. 1 has been developed to study the conduction and switching power losses. The proposed inverter is designed to deliver output power ($P_{out} = 1.9$ kW). A three-phase series resistive-inductive (23Ω , 3 mH/Phase) in star connection is used as load. The multi-Level dc link is determined as $V_{dc} = 75$ V, $2V_{dc} = 150$ V, and $V_{fix} = 4V_{dc} = 300$ V and the proposed staircase modulation technique at $M_a = 1$ is used to generate the appropriate switching gate signals. Three different types of power electronic components are selected to build the prototype of the proposed inverter power circuit as following: IGBT (HGTG20N60B3D) 600V/40A for the two-level bridge and CHB switches, IGBT (IRG4BC40W) 600V/20A for bi-directional switches, and Diode (RHRP1540) 400V/15A for embedded diodes in bi-directional switches and freewheeling diodes. The data sheets of the utilized semiconductor components can be easily accessed to obtain their characteristic curves.

Table - 5
Comparison of the Proposed N-Level Inverter with the Existing Inverters

Converter Type	NPC	FC	CHB	PROPOSED METHODS		
				1ST	2ND	3RD
Switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2\log_2(N-1)+12$
Gate Drivers	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2\log_2(N-1)+9$
Diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2\log_2(N-1)+12$
Clamping Diodes	$6(N-2)$	0	0	0	0	0
DC Supplies	$(N-1)$	$(N-1)$	$3(N-1)/2$	$(N-1)$	$1 + [(\sqrt{8N-15}-1)/2]$	$1 + \log_2(N-1)$
Clamping Capacitors	0	$3(N-2)$	0	0	0	0
Control Signals	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2\log_2(N-1)+9$

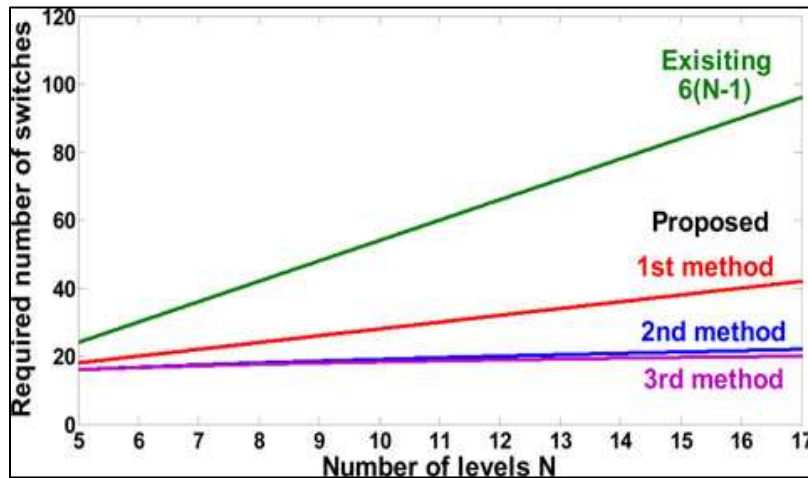


Fig. 8: Comparison of Required Number of Switches among Existing Inverters and the Proposed Topology

The mathematical models obtained for HGTG20N60B3D 600 V/40 A are given by

$$V_{on_IGBT1} = 1.418 e^{0.016t(t)} \quad (34)$$

$$E_{on_IGBT1} = (201.6 e^{0.04418t(t)} - 291.6 e^{-0.1265t(t)}) \times 10^{-6} \quad (35)$$

$$E_{off_IGBT1} = (323.3 e^{0.05125t(t)}) \times 10^{-6} \quad (36)$$

To simplify the losses calculation, a curve-fitting tool of MATLAB is used to approximate these curves by exponential equations [35]. While the mathematical models obtained for IRG4BC40W 600V/20A are given by

$$V_{on_IGBT\ 2} = 1.555 e^{0.0085371t(t)} \quad (37)$$

$$E_{sw_IGBT\ 2} = (0.340 e^{0.04472t(t)}) \times 10^{-3} \quad (38)$$

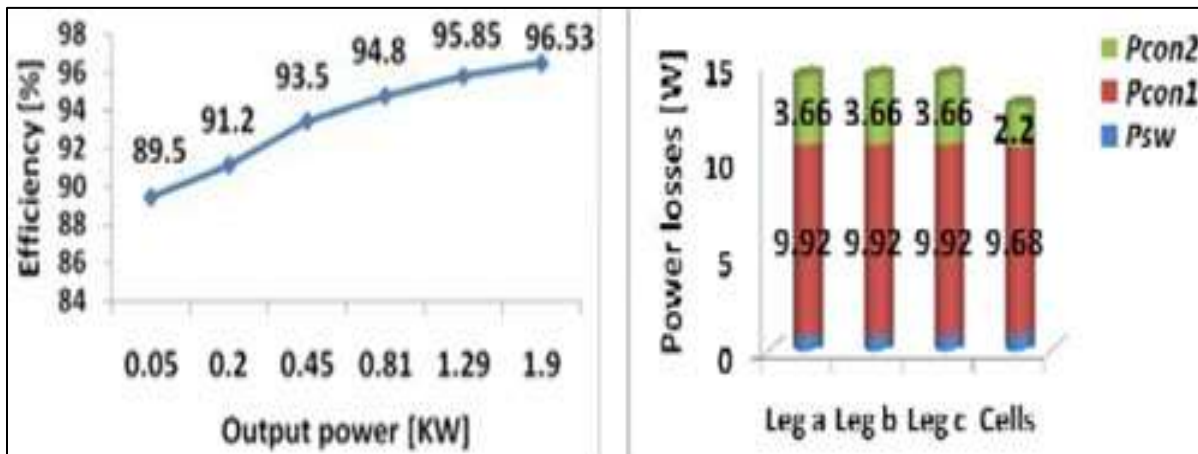
And finally, the mathematical models obtained for RHRP1540 400V/15A are given by

$$V_{on_diode} = 1.325 e^{0.006424t(t)} - 0.8571 e^{0.07183t(t)} \quad (39)$$

$$E_{rr_diode} = (15.7 e^{-0.002733t(t)} + 2.74 e^{-0.1413t(t)} - 3.162 e^{-0.05923t(t)} - 8 e^{-0.09452t(t)}) \times 10^{-6} \quad (40)$$

Hence, the conduction and switching power losses for the inverter switches and diodes can be estimated by substituting equations (34)–(40) into equations (28)–(33). When the input voltage is raised in small steps, the efficiency of the proposed inverter is estimated. Fig. 9(a) represents the estimated value of efficiency over a wide range of the output power. It is clear that the inverter's efficiency is directly proportional to the output power and reaches its optimized value of 96.53% at 1.9 kW. It is a result of more power being effectively transferred with respect to the power losses. Moreover, the distribution of power losses among the inverter's legs and the CHB cells are shown in Fig. 9(b). The distribution of power losses is attained during the operation of the proposed inverter to deliver $P_{out} = 1.287$ kW at step voltage $V_{dc} = 62.5$ V, $2V_{dc} = 125$ V, and $V_{fix} = 4V_{dc} = 250$ V. The generated power losses by the legs a, b, and c are almost equal and slightly higher than those generated by CHB cells. According to Fig. 9(b), 53.3% of the total value of power loss is experienced in the conventional two-level bridge, since 3×9.92 W in term of conduction power losses is generated by Q1–Q6. It is absolutely due to fact that the conduction power loss is directly proportional to the switching conduction time and the value of conducting current (for instance, Q1 and Q2 conduct the load current in 18 modes). Insignificantly conduction power losses are generated by the free whiling diodes (D1–D6). Further measurements show that $9.68 + 2.2$ W is the estimated value of the conduction power losses generated by CHB's switches and diodes. It is almost 21.3% of total power loss. The higher conduction power loss is experienced in T3 followed by T1, T4, and T2. The three bi-directional switches contribute to 19.6% of the total power loss as 3×3.66 W is the projected value of conduction power loss generated by S1–S6 and Da1–Dc2. Finally, it can be observed that a switching loss which is almost negligible is generated since the fundamental frequency is implemented. Additionally in order to assess the performance of the proposed inverter comparing with other types of the multi-level inverter, a five-level NPC multi-level inverter built by IRG4BC40W 600V/20A and RHRP1540 400V/15A semiconductor component types has been modeled and operated under the same conditions to the proposed inverter. The projected value of efficiency and power losses distribution of the NPC multi-level inverter are shown in Fig. 9(c) and (d). By comparing the proposed inverter's efficiency with the five-level NPC multi-level inverter's efficiency shows that the proposed inverter has a higher efficiency since the maximum estimated efficiency of the NPC multilevel inverter is 93.85%. The lower P_t generated by the proposed inverter comparing with P_t generated by the five-level NPC multilevel inverter is a result of the low conduction power losses and reduced number of power components. A lower voltage stress leads to a lower switching power loss. However, the more the switching devices, the higher the conduction power losses. At the same operating point $P_{out} \approx 1.287$ kW and compared with the estimated value of P_t proposed $= 3 \times 14.4 + 12.78 \approx 55.9$ W generated by the proposed inverter, the estimated value of P_t generated by the NPC multilevel inverter is two times higher. It is nearly P_t NPC $= 3 \times 37.5 \approx 112.5$ W. Moreover, the proposed inverter has been tested under different modulation indices ($M_a = 0.9, 1$, and 1.15). THD% of the output voltage can be calculated by

$$THD \% = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \times 100 \% \quad (41)$$



(a)

(b)

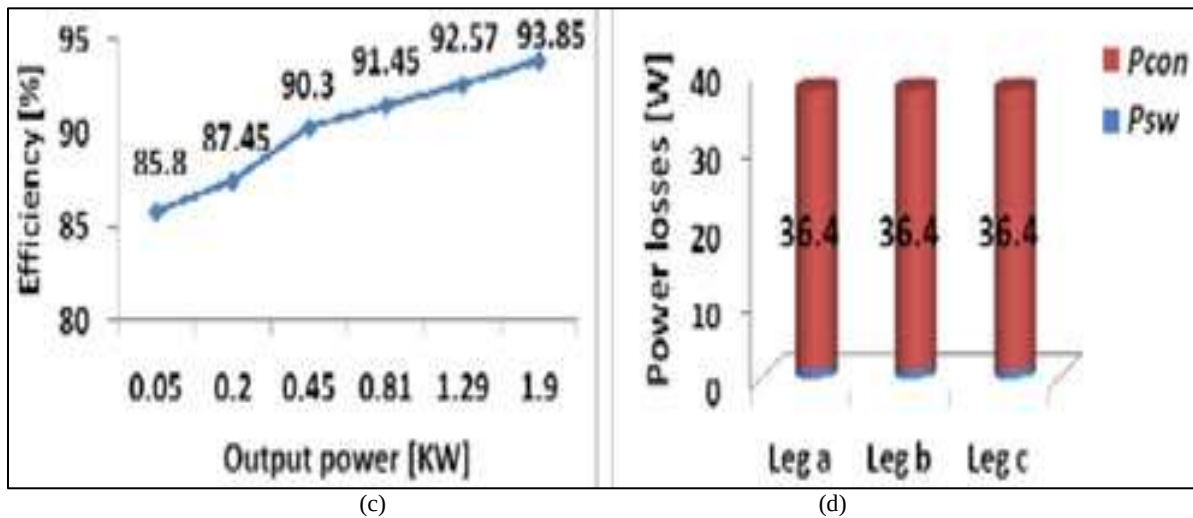


Fig. 9: Power loss and efficiency comparison. For the proposed inverter: (a) output power versus efficiency, (b) Pcon and Psw distribution among legs a, b, c, and CHB cells for $M_a = 1$ and $P_{out} = 1.287$ kW. For the NPC inverter: (c) output power versus efficiency and (d) Pcon and Psw distribution among legs a, b, and c for $M_a = 1$ and $P_{out} = 1.285$ kW

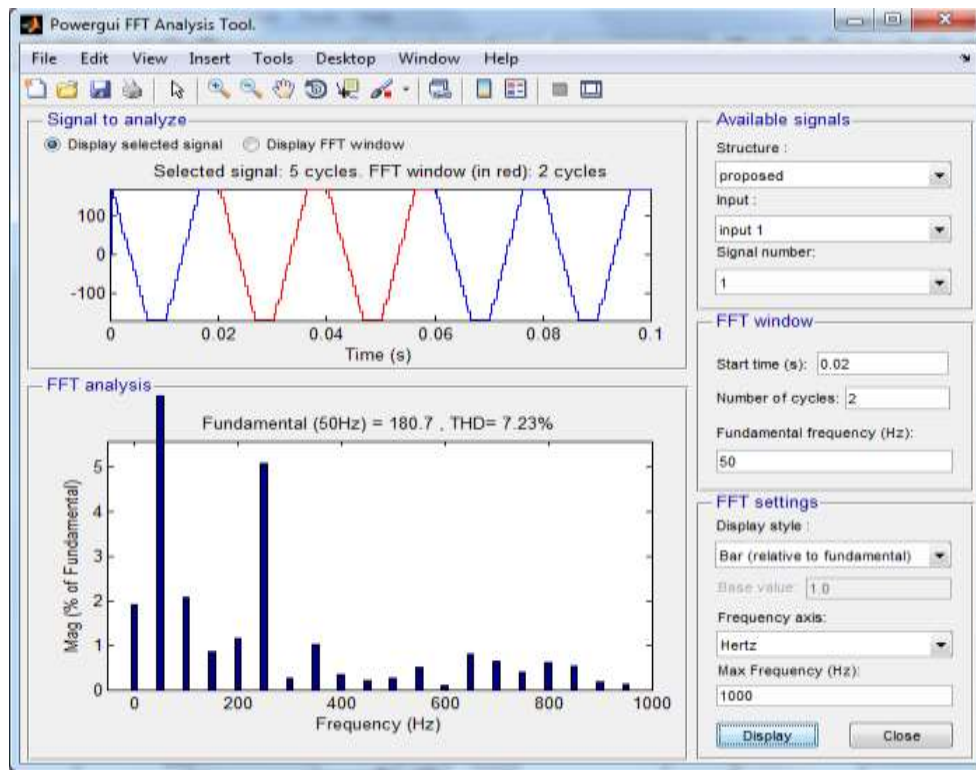


Fig. 10: NPC, FC, CHB, & Proposed Inverter: Line-To-Line Voltage THD% versus M_a

Table - 6
Proposed & the Existing Topologies Rating Requirements per Level N

Proposed Inverter	Main Bridge Q1-Q6 D1a-D2c	Bidirectional Switches S1 to S6 D1 to D6	Cascaded Half-Bridge Switches T11 to Tn2			Converter Type	NPC	FC	CHB
			1 st Method	2 nd Method	3 rd Method				
Component Voltage rating	$(N-1) V_{dc}$	$(N-2)V_{dc}$	V_{dc}	$n V_{dc}$	$2^{(n-1)} V_{dc}$	Switches Voltage Rating	V_{dc}	V_{dc}	V_{dc}
						Clamping Diode Voltage Rating	V_{dc}	0	0
Active Components current	IL	IL	IL	IL	IL	Clamping Diode Voltage Rating	0	V_{dc}	0
						Active Component Current	IL	IL	IL

Table - 7
Conducting Devices of the Proposed Inverter Phase a

Current	Conducting Devices Phase a. Fig. 1(a)	V_{ag}	Conducting Devices Phase a. Fig. 1(b)	V_{ag}
$I_a > 0$	Q1	$+4V_{dc}$	Q1	$+4V_{dc}$
	T1, T3, S2, Da2	$+3V_{dc}$	T1, T3, S2, Da2	$+3V_{dc}$
	Dz2, T3, S2, Da2	$+2V_{dc}$	Dz2, T3, S2, Da2	$+2V_{dc}$
	T1, Dz4, S2, Da2	$+V_{dc}$	T1, Dz4, S2, Da2	$+V_{dc}$
	D2, Da2	0	D2	0
$I_a < 0$	D1, Da1	$+4V_{dc}$	D1	$+4V_{dc}$
	Dz1, Dz3, S1, Da1	$+3V_{dc}$	Dz1, Dz3, S1, Da1	$+3V_{dc}$
	T2, Dz3, S1, Da1	$+2V_{dc}$	T2, Dz3, S1, Da1	$+2V_{dc}$
	Dz1, T4, S1, Da1	$+V_{dc}$	Dz1, T4, S1, Da1	$+V_{dc}$
	Q2	0	Q2	0

Where V_1 and V_k are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multi-level inverters have been tested under the same operating conditions. The aim of this test is to compare the proposed inverter with the existing inverters in term of THD%. Fig. 10 shows THD% of the line-to-line voltage for all inverters within specific range of modulation indices [0.9–1.15]. It can be seen that the THD% of all inverters are slightly different. The measured values of THD% for the proposed inverter are within a range of 8.4–13.25%. As a result, the proposed inverter basically adds the attractive aspects of the traditional two-level inverter such as less power electronic components, simple working principle, and minimum conduction power loss to the main advantages of the multi-level inverter such as low THD% and high output voltage quality.

VII. EXPERIMENTAL RESULTS

To ensure the feasibility of the proposed topology, the inverter concept was implemented and its prototype has been manufactured. During the hardware implementation, the inverter shown in Fig. 1 was tested under $V_{dc} = 22.5$ V in the first cell and $2V_{dc} = 45$ V in the second cell.

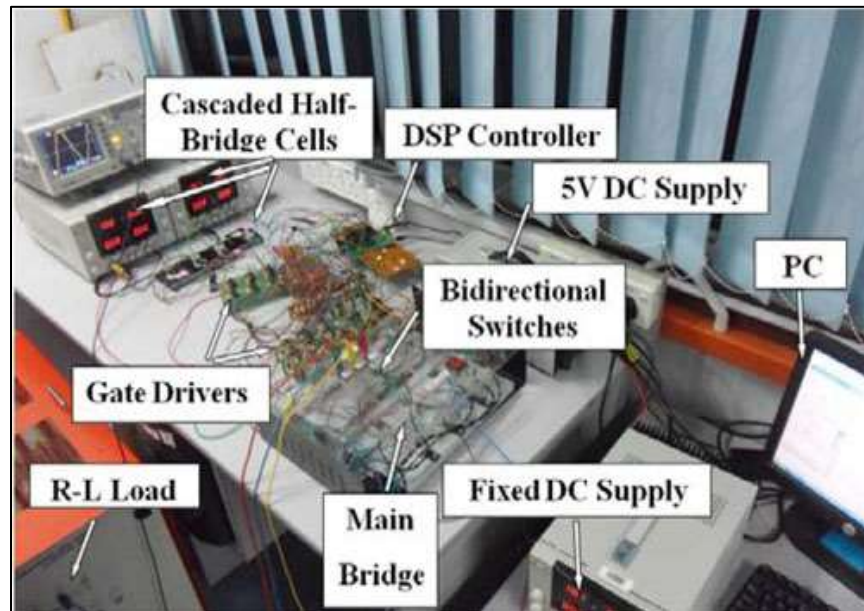


Fig. 11: Prototype of the Proposed Multilevel Inverter

Table - 8
Specifications of the Semiconductors

Six-Switched Bridge IGBTs (Q1-Q6)	HGTG20N60B3D, 40A, 600V
Half-Bridge Cells IGBTs (T1-T4)	HGTG20N60B3D, 40A, 600V
Bi-directional Switches IGBTs (S1-S6)	IRG4BC40W, 20A, 600V
Diodes	RHRP1540, 15A, 400V

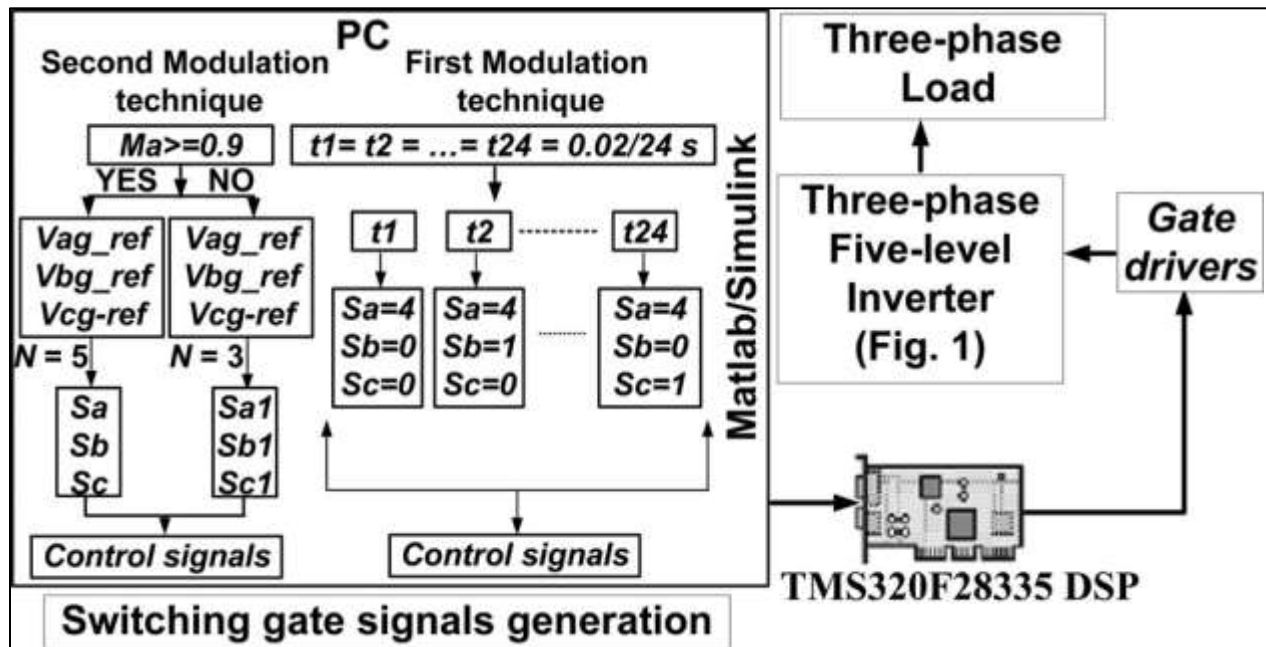


Fig. 12: Control Block Diagram

The magnitude of the fixed dc supply is determined as $V_{fix} = 4V_{dc} = 90$ V. A star connected fixed three-phase series resistive-inductive load (23Ω - $3mH$ /Phase) was used. In order to generate the appropriate switching gate signals, a DSP controller was used. The fundamental frequency $f = 50$ Hz staircase modulation technique was employed. In Fig. 11, the prototype of the proposed inverter is shown. It consists of the following components: personal computer, TMS320F28335 DSP controller, conventional six-switch bridge, fixed dc supply voltage, 13 gate drivers, three bi-directional switches, two half-bridge cells powered by 5 V dc supply, and fixed three-phase (R – L) load. The type of semiconductors used for the power circuit is provided in Table 8. Two modulation techniques are implemented to operate the proposed inverter as illustrated in the control block diagram (see Fig. 12). In the 1st modulation technique, the generation principle of the switching gate signals depends on time duration presented in Table 2, where the time duration of a cycle of the output waveform ($t = 1/50 = 0.02$ s) is divided into 24 equal time periods: $t_1=t_2=\dots=t_{24} = 0.02/24s$. During each period, the proposed inverter's switches are turned ON/OFF following the switching sequence illustrated in Table 2. In Fig. 13(a) and (b), there is an illustration of the switching gate signals of the four switches (Q1, S1, S2, and Q2) in leg of the main bridge and the four switches (T1, T2, T3, and T4) in the CHB circuit. The shapes of switching gate signals of switches in legs b and c are similar to those shown in Fig. 13(a) but they are shifted by $0.02/3$ and $0.04/3$ s, respectively. The operating frequencies f_{sw} of the proposed inverter's switches can be determined by means of the number of pulses per cycle as following: Q1–Q6 of the conventional bridge are turned ON/OFF at $f_{sw}=f = 50$ Hz, while the bidirectional switches (S1–S6) are turned ON/OFF at $f_{sw} = 2f = 100$ Hz. $f_{sw} = 6f = 300$ Hz and $f_{sw} = 4f = 200$ Hz are the operating frequency of the first cell switches T1 and T2 and the second cell switches T3 and T4, respectively. Fig. 13(c) depicts the inverter line-to-ground voltages V_{ag} , V_{bg} , and V_{cg} . It is clear that the controller manages to generate the appropriate switching gate signals that lead the inverter to output the desired waveform with five voltage steps. The inverter line-to-line voltages V_{ab} , V_{bc} , and V_{ca} waveforms with nine levels and the inverter line-to-neutral voltages V_{aN} , V_{bN} , and V_{cN} waveforms with 13 levels are shown in Fig. 13(d) and (e), respectively. In Fig. 13(f), the inverter terminal voltages V_{ao} , V_{bo} , and V_{co} reached their maximum value $3V_{dc}$ with seven voltage steps as planned. Based on shapes of V_{ag} and V_{og} , V_{og} takes three different voltage values and it repeats itself three times within a full cycle of V_{ag} as shown in Fig. 13(g). In Fig. 13(h), the experimental waveforms of load current and line-to-neutral voltage of phase are shown.

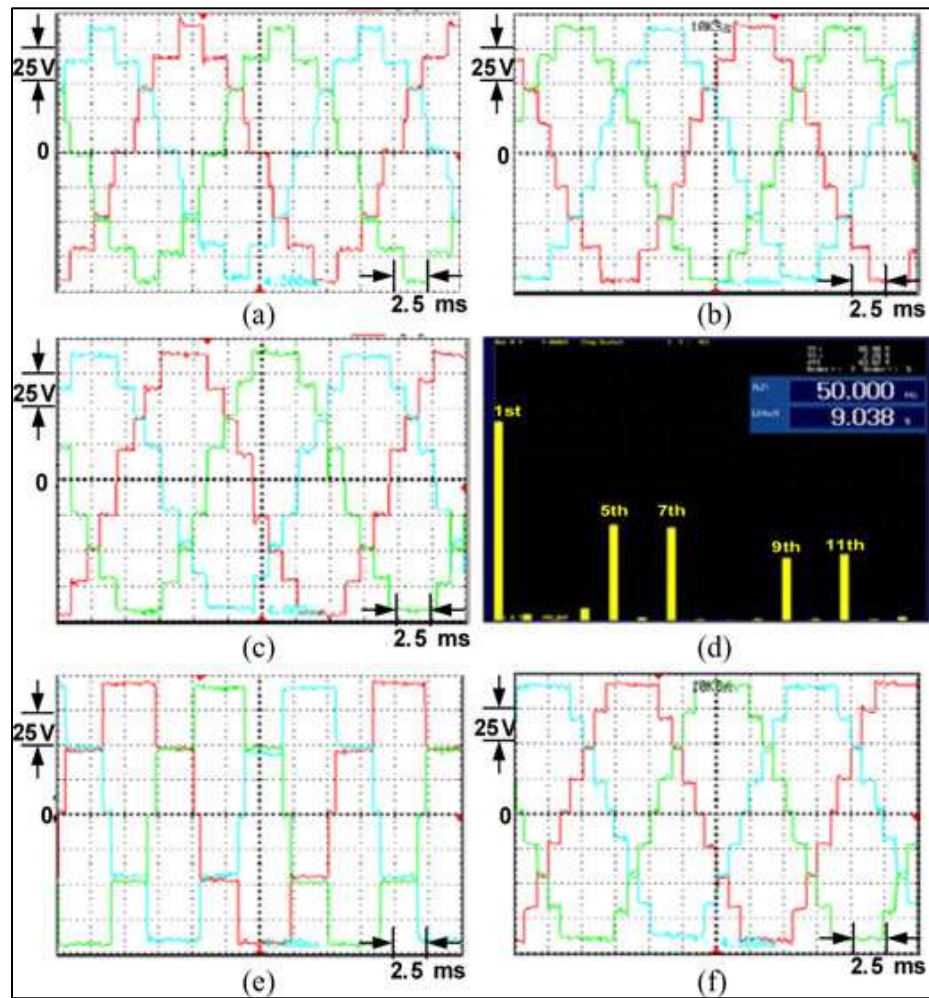


Fig. 14: (1) Three-line-to-line voltages at $M_a = 0.9$, (2) three-line-to-line voltages at $M_a = 1.05$, (3) three-line-to-line voltages at $M_a = 1.15$, (4) THD% at $M_a = 1.15$, (5) three-line-to-line voltages at $M_a = 0.8$, and (6) three-line-to-line voltages at $M_a = 1.3$

In order to investigate the performance of the proposed inverter at different modulation indices, the modulation procedure presented in Section III is executed. The proposed configuration was tested under different modulation indices $M_a = 0.9, 1$, and 1.15 . Fig. 14(1), (2), and (3) shows the inverter balanced line-to-line voltage waveforms. These voltage waveforms are similar to those obtained through simulation in Section III. THD% and the harmonic content of the line-to-line voltage V_{ab} at $M_a = 1.15$ are shown in Fig. 14(4). The graph contains the fundamental frequency component followed by 14 harmonic components. Due to the symmetry attained in the inverter output line-to-line voltage, all the even harmonic components are almost eliminated. Also, the triplen harmonic components such as 3rd, 9th, and 15th are eliminated. A lower harmonic components lead to a lower THD%. The measured THD% is found around 9.038%. The measured (rms) value of the fundamental frequency component of the line-to-line voltage waveform V_{ab} is 63.61V. It is nearly $1.15 \times (0.612 \times 4V_{dc})$ where $0.612 \times 4V_{dc} = 55.08$ V is the maximum (rms) value of the fundamental frequency component at $M_a = 1$. It can be seen that the (rms) value of the fundamental frequency component shown in Fig. 14(4) is improved by 15% at low THD%. The Fig. 15. Experimental results of (a) output power versus efficiency for the proposed inverter and (b) line-to-line voltage THD% versus M_a for $V_{dc} = 75$ V. The normalized value of the larger harmonic component (5th) is $3.42/63.61 = 0.053$. By applying staircase modulation with selective harmonic, the present harmonic components such as 5th, 7th, and 11th can be eliminated. It is worth noting that the estimation of optimal switching angles is not the objective of this paper. Decreasing the modulation index to $M_a = 0.8$ results in three positive levels (0, +2V_{dc}, and +4V_{dc}) in the inverter output line-to-line voltage waveforms as shown in Fig. 14(5). Such decreasing makes the proposed configuration operates as a traditional three-level inverter. The over modulation happens when the proposed inverter is operated at $M_a > 1.15$. Fig. 14(6) represents the experimental voltage waveforms of the proposed inverter at $M_a = 1.3$. Further studies were conducted to verify the efficiency of the proposed inverter at the fixed R – L load. The efficiency took different values at different voltages supplied from the dc link as represented in Fig. 15(a). 1.9 kW of power was reached at modulation index $M_a = 1$. However, V_{dc} took the maximum value of 75 V. Since $V_{fix} = 4V_{dc}$ and during the testing the maximum dc value was supplied from V_{fix} that increased upto 300 V, the inverter's efficiency can be calculated based on the measured data as follows:

$$\eta\% = \frac{P_{out}}{P_{in}} \times 100 \quad (42)$$

Where Pin and Pout are the inverter input and output power, respectively. The digital meter was utilized to measure Pin and Pout. The efficiency takes values around 88% under low power conditions. However, better efficiency is attained at higher power as 95.2% is the measured efficiency at 1.9 kW. By comparing the measured efficiency shown in Fig. 15(a) with the calculated efficiency shown in Fig. 9(a), it can be seen that the measured efficiency is slightly lower than calculated. It is due to supplementary loss generated by cable resistance and measurements accuracy. If this further loss is considered and added, both measured and calculated efficiencies show a close agreement. Hence, the proposed inverter is promising configuration that may serve in many applications. The variation of THD% with the modulation index for the inverter line-to-line output voltage is shown in Fig. 15(b). This demonstrates that THD% is inversely proportional to the modulation index Ma. In other words, a lower THD% in the output voltage is experienced at higher modulation index.

VIII. CONCLUSION

A new topology of the three-phase five-level (multi-level) inverter was introduced. The proposed configuration was obtained by reducing the number of power electronic components used. Thus, the proposed topology results in decrease in cost and installation area. The fundamental frequency staircase modulation topology was easily engaged and showed high flexibility and simplicity in control. Besides, the proposed configuration was extended to N-level with different methods. Furthermore, the method employed to determine the magnitudes of the dc voltage supplies was well executed. In order to validate the performance of the proposed multi-level inverter, the proposed configuration was simulated and its prototype was manufactured. The obtained simulation and hardware results met the desired output. Henceforth, subsequent work in the future may include an extension to higher level with other recommended methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation (PWM) technique can be also executed.

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