Design and Implementation of FPGA Controlledbuck-Boost Converter for Wide Range of Input Voltage

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Abstract— Dead time in a synchronous controlled dc–dc converter adversely affect the stability of a four-switch non inverting buck-boost converter. The pulse-skipping phenomenon occurs in the mode-transition region near the boundary between the step-down and step-up regions, and this phenomenon leads to an unstable output voltage and an unpredictable output voltage ripple. These results may damage the entire power system and application system. This paper proposes an enhanced Duty Cycle-Overlap control technique for a digitally controlled non inverting buck-boost converter. The proposed technique offers two duty cycles limitations for various conditions in the mode-transition region and ensures the stability of the digital controller and output voltage. Moreover, this technique involves combining the duty cycles of both step-down and step-up modes for deriving an accurate value of the output voltage.

Key words: Digital control, pulse-skipping, mode-transition technique, non-inverting buck-boost converter, FPGA

I. INTRODUCTION

Currently, electronic portable devices have become a major part of modern life and the consumer market. However, the energy capacity of commonly used lithium-based batteries is limited. Therefore, high efficiency power management has become increasingly critical regarding portable devices. Given the highly variable nature of batteries, the systems require to supply the voltages both higher (e.g. special white LED applications) and lower (e.g., audio applications) than the battery voltage. On the other hand, the necessary voltage level can vary for a specific part of a device, such as in radio frequency power amplifiers (RFPAs). In these situations, a dc-dc converter is required that can operate in both step-down and step-up regions. Previously, dc-dc converters have been created that can achieve both step-down and step-up functionality, such as the K-Y buck-boost converter [1, 2], cascade buck and boost converter [3], and non-inverting buck-boost converter [4]. In this paper, the non-inverting buck-boost (NIBB) converter was chosen as the basis for the topology of a power stage, because it uses non-inverting output voltage and requires fewer components than the other types of the converter.

II. FOUR SWITCH BUCK-BOOST CONVERTER

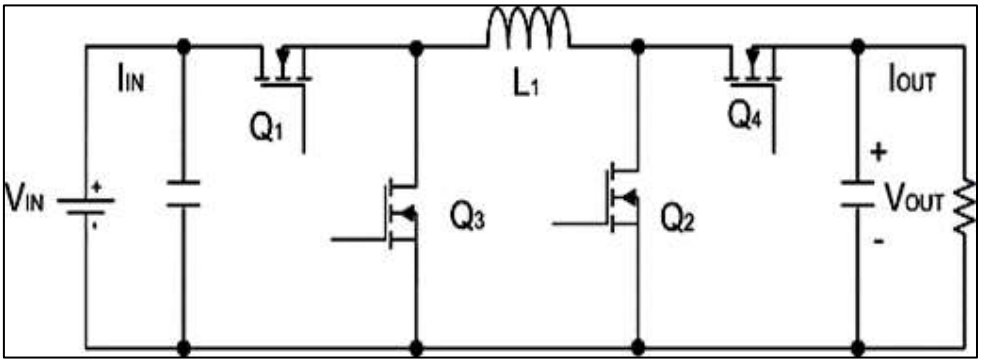

Fig. 1: Four switch buck-boost converter

Fig.1 shows a four-switch NIBB (Non- Inverting Buck-Boost) converter. The power stage of the converter comprises four switches, an inductor, and an output capacitor, whereas normal converters, such as buck or boost converters, used in portable devices contain only two switches. The conventional operation of NIBB converters results in significantly higher inductor current compared to normal buck or boost converters. The efficiency of NIBB converters can be improved by designing them to operate in a buck mode or boost mode, depending on whether the output voltage is higher or lower than the input voltage.

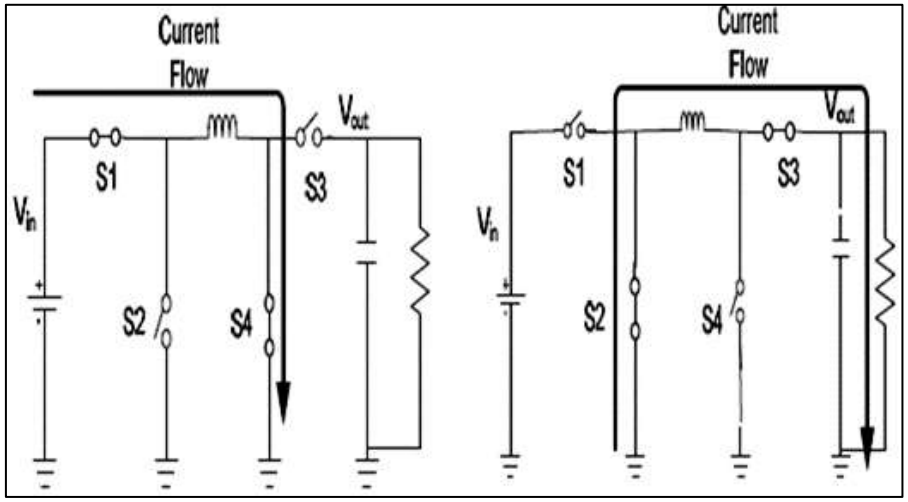

Fig. 2: Buck-Boost mode operation

The four-switch buck-boost converter (Figure 2) operates in buck-boost mode. In this operation mode, all four switches (S1, S2, S3 and S4) are switching and generating switching loss in each switching period. Moreover, all four switches – as well as inductor L1 – see a current stress of IIN+IOUT with inductor ripple current neglected, which results in a large conduction loss. Such large switching and conduction losses in buck-boost mode make the buck-boost converter not as efficient as a buck or boost converter.

A major pulse-skipping problem arises between the buck and boost mode transition when Vin is highly close to Vout. Therefore, providing an additional mode between the buck and boost modes is necessary to eliminate the pulse-skipping problem. Various mode-transition methods have been proposed for removing the pulse-skipping phenomenon. Duty Cycle-Overlap control is the most frequently used structure for generating the required output voltage.

III. DUTY CYCLE OVERLAP CONTROL

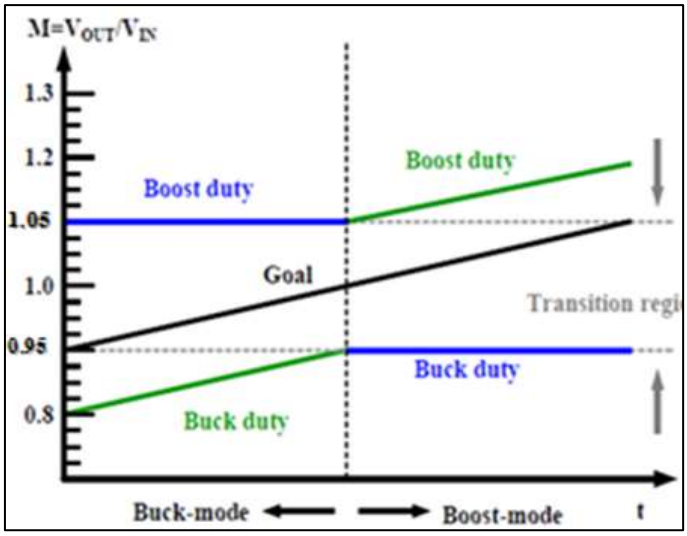

Fig. 3: Duty cycle limitation in mode transition region

To ensure a stable output voltage, the occurrence of pulse skipping must be avoided. The output does not exhibit jitters or oscillations if the D is maintained at an appropriate value. According to a previous study [5], Ds that resulted in pulse skipping were considerably close to 100% or 0%; therefore, the output of the converter was poor near the transition point in both the buck and boost modes. This instability can be avoided when the duty-cycle is exactly equal to the buck-mode at 100% (95%) or the boost-mode at 0% (5%). No switch in the power stage was the activated or deactivated during this operation, meaning that the duty-cycle was not affected by any non-ideal factors. After a control scheme is identified, the limits on the duty cycle of the buck and boost operations should be set to avoid the pulse-skipping phenomenon. In a digital controller, the only parameter affecting the extent of the transition region is the dead time. Therefore, the dead time becomes the main consideration for setting the limits of the transition region.

IV. DIGITAL CONTROLLED NIBB CONVERTER

The NIBB converter can be divided into two parts. The digital part comprises a digital PID compensator and a mode detector for determining various limits in the enhanced duty cycle-overlap control. The other part involves a PCB containing power

MOSFETs [7], gate drivers, Comparator IC for A/D conversion, and all the passive components. Fig 4 shows the control scheme block diagram.

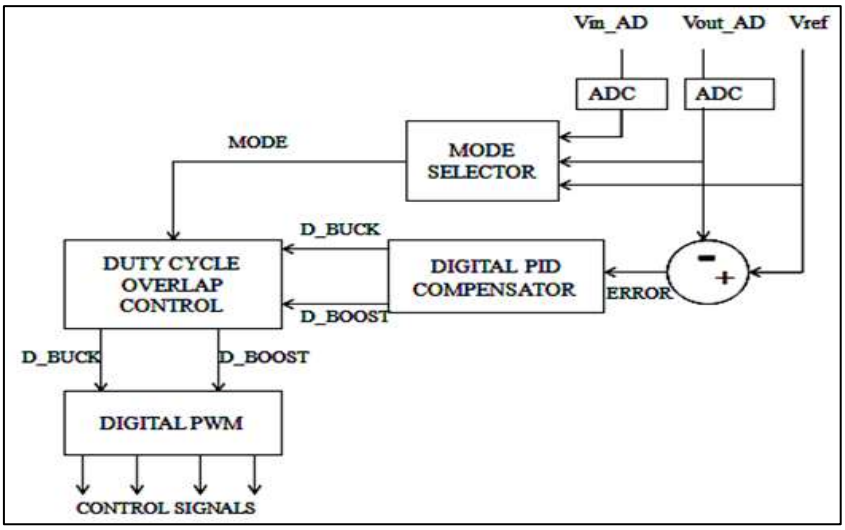

Fig. 4: Control block

A. Mode Selector Block and Duty Cycle Overlap Control Block:

In the control system, the mode detector block samples the input and output voltages for determining the operating mode of the converter. The proposed NIBB converter will be having 4 modes of operation: normal buck, boost, step-down mode-transition, and step-up mode-transition modes. When the converter system operates in the normal buck or boost mode, the enhanced duty cycle-overlap control block is bypassed. When it operates in the step-up and step-down mode-transition region, the enhanced duty cycle-overlap control block modifies the output signals of the compensator by different limits. For example, when the converter operates in the step-down part of the transition region, the transition block limits the boost mode duty cycle to a minimum value of 10%. Similarly, when it operates in the step-up part of the transition region, the control block limits the buck mode duty cycle to a maximum value of 90%.

B. Digital PID Compensator:

PID compensator will decide the duty cycle according to the error between required reference and output voltage. In this project a look-up-table based PID compensator is used for achieving a quick response and using a low number of logic gates.

C. Digital PWM Block:

According to the duty cycle switching signal for the four switches are provided by the DPWM block. Necessary dead time conditions are also incorporated with the switching signal in this block.

D. ADC:

The ADC is a common analog building block and almost always is needed when interfacing digital logic like that in an FPGA or CPLD, to the "real world" of analog inputs.

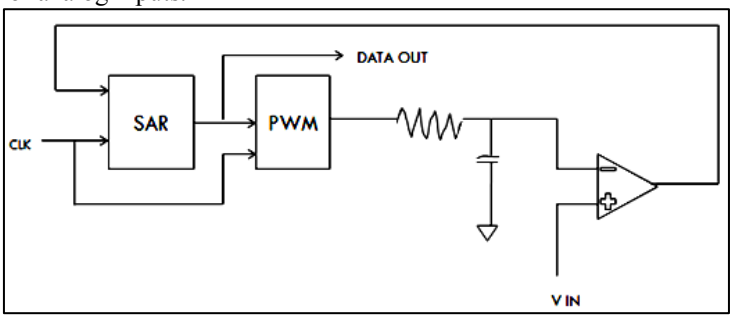

Fig. 5: SAR based ADC

In this project a SAR based ADC is using. A successive approximation ADC works by using a digital to analog converter (DAC) and a comparator to perform a binary search to find the input voltage. A PWM module is used as DAC which with provide more precise value.

V. EXPERIMENTAL RESULTS

The NIBB converter can be divided into two parts. The digital part comprises a digital PID compensator and a mode detector for determining various limits in the enhanced duty cycle-overlap control. The other part involves a PCB containing power MOSFETs, gate drivers(TLP250), comparator IC, and all the passive components. The input voltage is 3-9 V, the output voltage is 5 V, and the switching frequency is fixed at 50 KHz. The digital controller of the experimental system was realized using a

field-programmable gate array (FPGA) development kit. Simulation of converter have been first done on matlab simulink. Fig 6 shows the prototype.

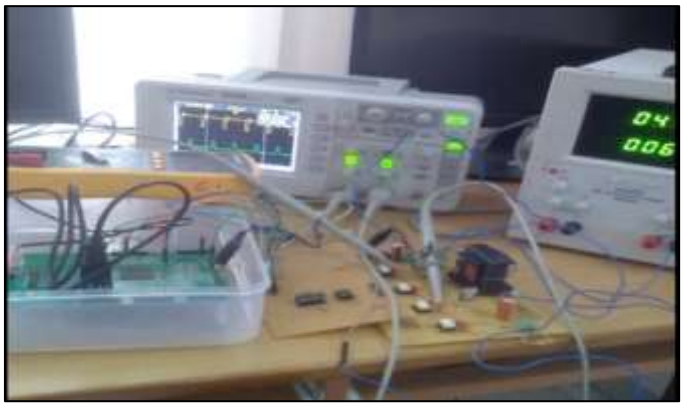

Fig. 6: Experimental environment

First the power stage is tested for gate pulses along with deadband. Deadband is taken as 1 percent of the total time period. Figs. 7 and 8 show the results of the converter operation in the normal buck mode and boost mode. Specifically, Fig. 7 presents the results for the buck mode operation at input and output voltages of 7V and 5V, respectively, and Fig. 8 shows the results of the boost mode operation at input and output voltages of 4V and 5V, respectively. To verify the concept proposed in this paper, the input voltage was set at 5.5V; at this voltage, the system operates in the step-down part of the mode-transition region. The input voltage was also set at 4.5V to obtain results for the step-up part. Figs. 9 and 10 illustrate the steady-state results for the mode-transition region.

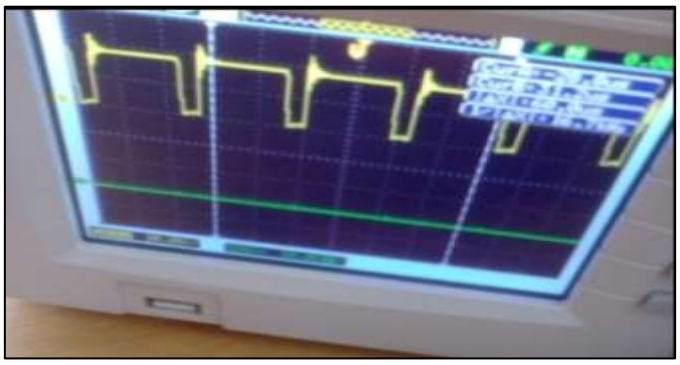

Fig. 7: Result of normal buck mode

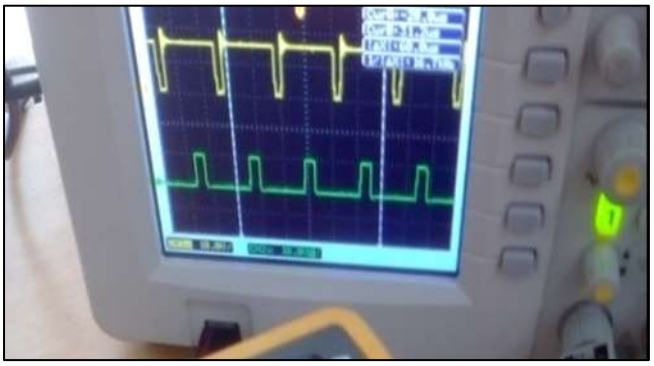

Fig. 8: Result of normal boost mode

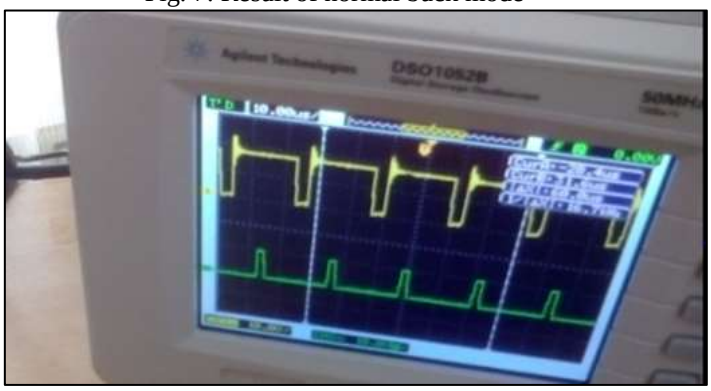

Fig. 9: Result of step down mode transition region

Fig. 10: Result of step up mode transition region

Input Voltage	Output Voltage	Mode	Buck Duty Cycle	Boost Duty Cycle
7 V	5.1 V	Buck Mode	71%	0%
4 V	4.48 V	Boost Mode	100%	20%
5.3 V	5.13 V	Step-Down Transition Mode	85%	10%
4.7 V	5.07 V	Step-Up Transition Mode	90%	15%

Table 1: Results of the studies

VI. CONCLUSION

The proposed enhanced duty cycle-overlap control method can be applied to converters with any specifications, regardless of the dead time or switching frequency. This work can be implemented in any synchronous NIBB converter provided that the duty cycle limits are appropriately defined. The system involving only one dual-output digital compensator and the enhanced

duty cycle-overlap control technique provides a stable and accurate output voltage and a smooth mode-transition process, preventing the occurrence of the pulse-skipping phenomenon.

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